1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0000891242	PRODUCTION RELEASED	2010-04-13

K74 MLB

LAST_MODIFIED=Tue Apr 13 17:17:57 2010

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 13 17:17:57 2010

DRAWING TITLE: SCH,K74,MLB

Apple Inc.

DRAWING NUMBER: 051-8337
SIZE: D
REVISION: A.0.0
BRANCH:
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SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
System Block Diagram

Apple Inc.

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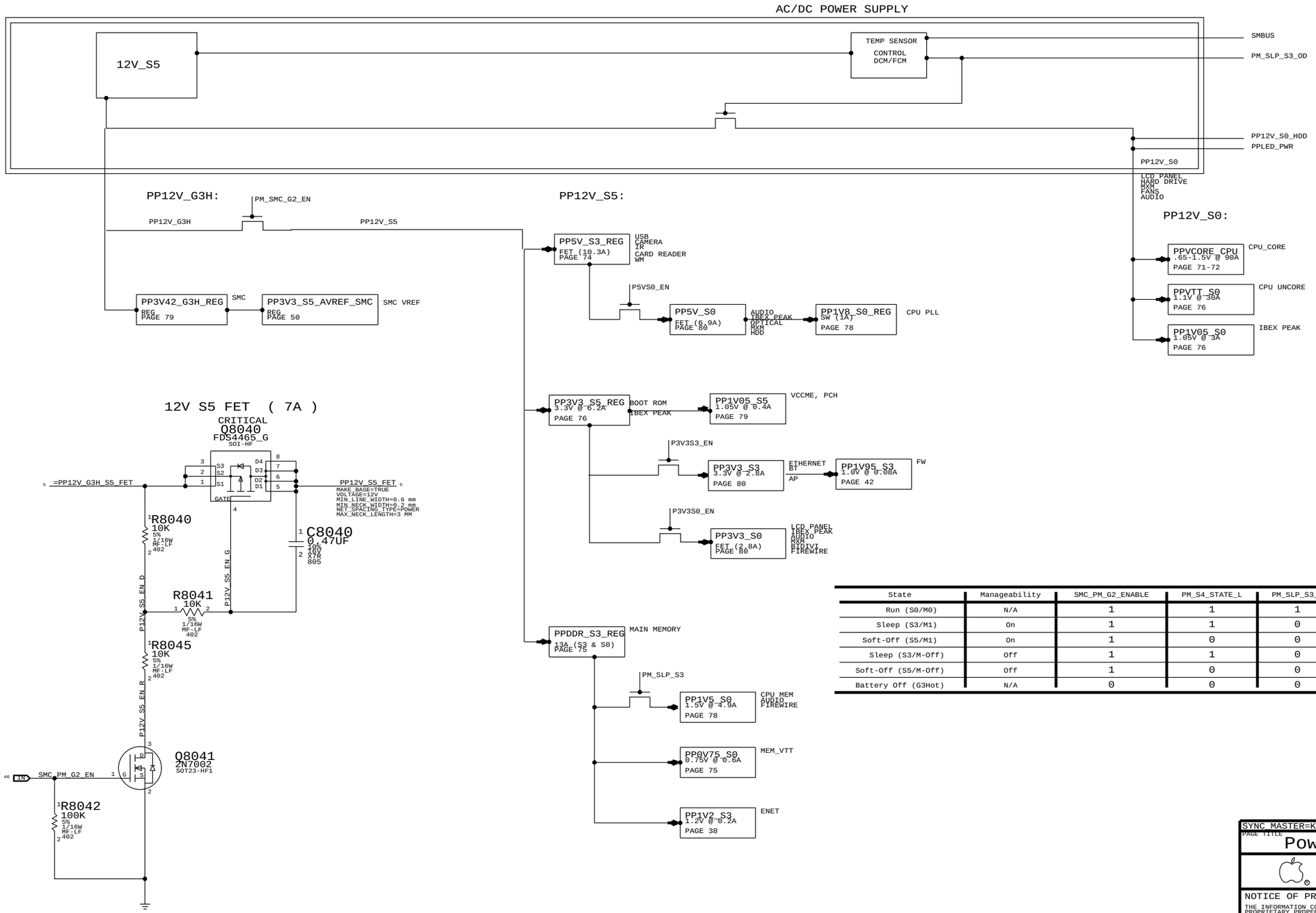

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1107	PCBA,MLB,DEV,K74	DEVELOPMENT,DEV_GROUP
639-0698	PCBA,MLB,K74,2.93GHZ,CKD	K74,2P93GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0707	PCBA,MLB,K74,3.06GHZ,CKD	K74,3P06GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0808	PCBA,MLB,K74,3.20GHZ,CKD	K74,3P20GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0695	PCBA,MLB,K74,3.46GHZ,CKD	K74,3P46GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0991	PCBA,MLB,K74,3.60GHZ,CKD	K74,3P60GHZ_CKD_CPU,BASIC,CLARKDALE_73W
639-0694	PCBA,MLB,K74,2.53GHZ,LFD	K74,2P53GHZ_LFD_CPU,BASIC,LYNNFIELD_82W

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,MXM,XDP_CPU_BPM,PCH_VRM,BUF_CLK,HUB_USX2061,FW_TI_INT_VREG,BCM5764M,SD_USB,METAL_IO,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_1V5_SENSE,VREFMRGN

CPU SOCKET & ILM SUB-BOMS

ALTERNATE SOCKET VENDORS MUST USE MATCHING ILM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX,K74	ILM	CRITICAL	MOLEX_SOCKET
511S0069	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	FOXCONN_SOCKET
604-1246	1	ASSY,PURCHASED,ILM,MOLEX,K74	ILM	CRITICAL	FOXCONN_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
607-6694	SUB ASSY,CPU SOCKET,K74,MOLEX	MOLEX_SOCKET
607-6693	SUB ASSY,CPU SOCKET,K74,FOXCONN	FOXCONN_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-6694	1	MOLEX CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-6693	607-6694		SKT_ILM	FOXCONN ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

RAW: 335S0663

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3828	1	IC,IBEX PEAK PRQ,DESKTOP,FCBGA,PCH,P42S	U1800	CRITICAL	
359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
341T0230	1	IC,EFI BOOTROM,K74/K75	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
343S0493	1	IC,BCM5764M,ENET,8X8	U3900	CRITICAL	BCM5764M
343S0494	1	IC,BCM57765A,ENET&SD,8X8	U3900	CRITICAL	BCM57765
341T0269	1	ENET 1MBIT FLASH,CII,K74/K75	U3990	CRITICAL	BCM5764M
341T0246	1	ENET 1MBIT FLASH,CIV,K74/K75	U3990	CRITICAL	BCM57765

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3837	1	CKD,Q3GR,QS,2.93,73W,1333,C2,4M,LGA	CPU	CRITICAL	2P93GHZ_CKD_CPU
337S3912	1	CKD,SLBTD,PRQ,3.06,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P06GHZ_CKD_CPU
337S3911	1	CKD,SLBUD,PRQ,3.20,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P20GHZ_CKD_CPU
337S3900	1	CKD,SLBLT,PRQ,3.46,73W,1333,C2,4M,LGA	CPU	CRITICAL	3P46GHZ_CKD_CPU
337S3910	1	CKD,SLBTM,PRQ,3.60,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P60GHZ_CKD_CPU
337S3862	1	LFD,Q3C6,QS,2.53,82W,1333,B1,8M,LGA	CPU	CRITICAL	2P53GHZ_LFD_CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3898	337S3912	3P06GHZ_CKD_CPU	CPU	C2,PRQ,3.06 GHZ CKD

K74 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8337	1	SCH,MLB,K74	SCH1		
820-2784	1	PCBF,MLB,K74	MLB1		
341T0231	1	IC,SMC,K74	U4900	CRITICAL	K74

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0339	197S0179		Y4190	FIREWIRE OSCILLATOR
128S0298	128S0293		C1670,C7260,C7444	

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: BOM Configuration

Apple Inc.

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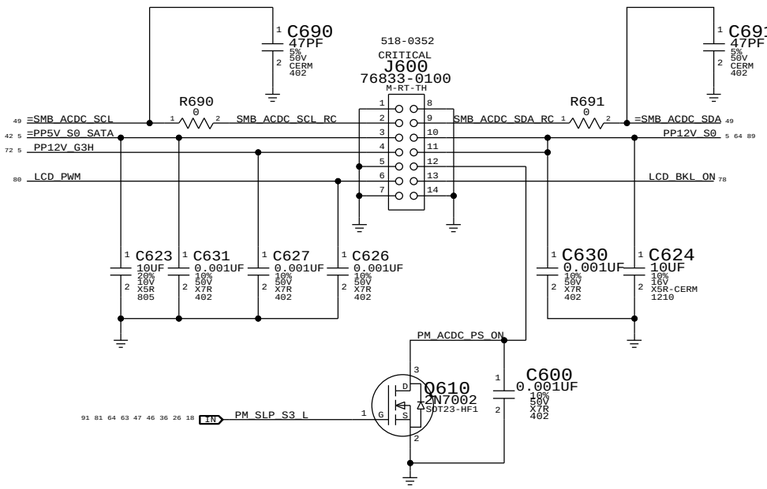
EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.



"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_DDR_FET 26
→ =PP0V75_S0_MEM_VTT_B 31
→ =PP0V75_S0_MEM_VTT_A 30

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVCORE_S0_CPU_REG 65 66 67
→ =PPVCORE_S0_CPU 12 15

PPVTT_S0
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_CPU_REG 68
→ =PPVTT_S0_PCH_VCC_DMI 21 23
→ =PPVTT_S0_XDP 24
→ =PPVTT_S0_PCH_VCCP_CPU 21 23
→ =PPVTT_S0_CPU 10 12 15 47 65

PP1V5_CPU_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP1V5_CPU_MEM 10 12 15 29

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V5_S0_FET 50 73
→ =PP1V5_S0_AUD_DIG 56
→ =PP1V5_FWRS0_FWXIO 39
→ =PP1V5_S0_CK505 25
→ =PP1V5_S0_MINI 33

PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V8_S0_REG 71
→ =PP3V3R1V8_S0_PCH_VCCPNAND 21 23
→ =PP1V8R1V5_S0_PCH_VCCVRM 23
→ =PP1V8_S0_CPU_PLL 12 15 64

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S0_FET 73
→ =PP3V3_S0_PCH 17 20 23 69
→ =PP3V3_S0_FAN 53 54
→ =PP3V3_S0_PCH_VCCADAC 16
→ =PPSPD_S0_MEM_A 30 47
→ =PPSPD_S0_MEM_B 31
→ =PP3V3_S0_VRD 65
→ =PP3V3_S0_AUDIO 56 58 59 60 61 62
→ =PP3V3R1V5_S0_PCH_VCCSUSHDA 21 23
→ =PP3V3_S0_SMBUS 49
→ =PP3V3_S0_SMC_LS 47 51
→ =PP3V3_S0_SMBUS_SMC_0_S0 49
→ =PP3V3_S0_SMBUS_SMC_B_S0 49
→ =PP3V3_S0_SMBUS_SMC_MGMT 49
→ =PP3V3_S0_DPCONN 81
→ =PP3V3_S0_TSENS 52
→ =PP3V3_S0_MXM 64 74 75
→ =PP3V3_S0_ODD 42
→ =PP3V3_S0_SATALED 17 42
→ =PP3V3_S0_SMC 47 50
→ =PP3V3_S0_PWRCTL 63 64 73
→ =PP3V3_S0_PCH_VCC3_3_CORE 21 23
→ =PP3V3_FW_FWPHY 39 40 41
→ =PP3V3_FWRS0_FWXIO 39
→ =PP3V3_S0_DP 78 79 80
→ =PP3V3_S0_PCH_VCC3_3_PCI 21 23
→ =PP3V3_S0_CK505 25
→ =PP3V3_S0_PCH_GPIO 19
→ =PP3V3_S0_PCH_STRAPS 14
→ =PP3V3_S0_PCH_VCC3_3_SATA 21 23
→ =PP3V3_S0_RSTBUF 27
→ =PP3V3_S0_ENETPHY 37
→ =PP3V3_S0_PCH_PM 27
→ =PP3V3_S0_SMBUS_SMC_BSA 49
→ =PP3V3_SM_PCH_VCC_ME 21 23
→ =PP3V3_S0_SDCARD 45
→ =PP3V3_S0_CPU_VTT_VREG 68

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S0_FET 73
→ =PP5V_S0_AUDIO 56
→ =PP5V_S0_SATA 5 42
→ =PP5V_S0_MXM 74
→ =PP5V_S0_VRD 65
→ =PP5V_S0_ISENSE 50
→ =PP5V_S0_P1V8_VREG 71
→ =PP5V_S0_PCH 23
→ =PP5V_S0_CPU_VTT_VREG 68
→ =PP5V_S0_LPCPLUS 48
→ =PP5V_S0_PCH_CORE_VREG 69
→ =PP5V_S0_DP_AUX_MUX 80

PP1V05_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_S0_REG 69
→ =PP1V05_S0_PCH_VCCADPLL 16
→ =PP1V05_S0_PCH_VCCIO_DMI 21 23
→ =PP1V05_S0_PCH_VCCIO_SATA 17 21 23
→ =PP1V05_S0_PCH_VCCIO_PCIE 17 18 21 23
→ =PP1V05_S0_PCH_VCC_CORE 21 23
→ =PP1V05_S0_PCH_VCCIO_USB 21 23
→ =PP1V05_S0_CK505 25
→ =PP1V05_SM_PCH_VCC_ME 21 23

PP1V05_SM_PCH_LAN
MAKE_BASE=TRUE
VOLTAGE=1.05V
→ =PP1V05_SM_PCH_VCC_LAN 21 23
UNUSED, GROUNDED ON CSA 24

PP0V75_S0
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_DDR_LDO 71
→ =PP0V75_S0_MEM_VTT_S0FET 26

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP12V_S0_FAN 53 54
→ =PP12V_S0_AUDIO_SPKRAMP 58 59
→ =PP12V_S0_VRD 65
→ =PPV_S0_MXM_PWR 50
→ =PP12V_S0_LCD 78
→ =PP12V_S0_PCH_CORE_VREG 69
→ =PP12V_S0_CPU_VTT_VREG 68
→ =PP12V_S0_PWRCTL 64
→ =PP12V_S0_SENSE 51
→ =PP12V_S0_FW 41

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V5_S3_REG 71
→ =PP1V5_S3_MEMRESET 26
→ =PPDDR_S3_S0FET 73
→ =PP1V5_S3_MEM_A 28 29 30
→ =PP1V5_S3_MEM_B 28 29 31

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S3_FET 73
→ =PP3V3_S3_BT 44
→ =PP3V3_S3_SMBUS_SMC_A_S3 49
→ =PP3V3_S3_MINI 33
→ =PP3V3_S3_PWRCTL 64 73
→ =PP3V3_S3_MEMRESET 26
→ =PP3V3_S3_USB_HUB 34 35
→ =PP3V3_S3_USB_RESET 34
→ =PP3V3_S3_SDCARD 44 45
→ =PP3V3_S3_VREFMRGN 28
→ =PP3V3_S3_ENETFET 36

PP5V_S3
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S3_REG 70 92
→ =PP5V_S3_USB 43
→ =PP5V_S3_S0FET 73
→ =PP5V_S3_CAMERA 44
→ =PP5V_S3_IR 44
→ =PP5V_S3_PWRCTL 63
→ =PP5V_S3_MEMRESET 26
→ =PP5V_S3_DDR_VREG 71

ENET RAILS

PP3V3_ENET
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_ENET_FET 36
→ =PP3V3_ENET_PHY 36 37 45

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S5_REG 5 70
→ =PP3V3_S5_PCH 17 18 23
→ =PP3V3_S5_PCH_GPIO 19
→ =PP3V3_S5_ROM 48 55
→ =PP3V3_S5_PCH_VCCSUS3_3_USB 21 23
→ =PP3V3_S5_PWRCTL 10 63 64
→ =PP3V3_S5_S3FET 73
→ =PP3V3_S5_S0FET 73
→ =PP3V3_S5_PCH_STRAPS 14
→ =PP3V3_S5_CPURESET 10
→ =PP3V3_S5_XDP
→ =PP3V3_S5_LPCPLUS 48

PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S5_LDO 70
→ =PP5V_S5_PCH 23

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP12V_S5_FET 3
→ =PP12V_S5_DDR_VREG 71
→ =PP12V_S5_P3V3S5_VREG 70
→ =PP12V_S5_P5VS3_VREG 70
→ =PP12V_S5_PWRCTL 64 73

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V42_G3H_REG 72
→ =PP3V3_S5_RTC_D 27
→ =PP3V3_G3H_SMC 46 47
→ =PP3V3_G3H_SMCUSBMUX 43
→ =PPVIN_S5_SMCVREF 47
→ =PP3V3_G3H_LPCPLUS 48

PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP12V_G3H_S5_FET 3

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM
→ =PPVAXG_S0_CPU 12

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

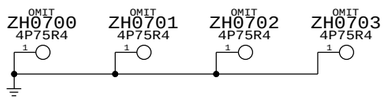
PAGE TITLE: Power Conn / Alias

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 6 OF 110
SHEET: 5 OF 92

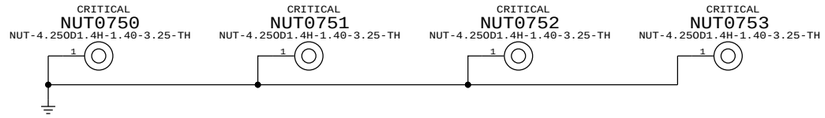
CPU Heatsink

4mm Plated Holes (998-0850)



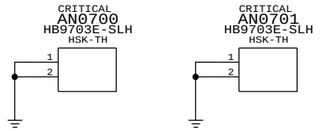
DIMM CONNECTOR NUTS

Nuts (805-9582)



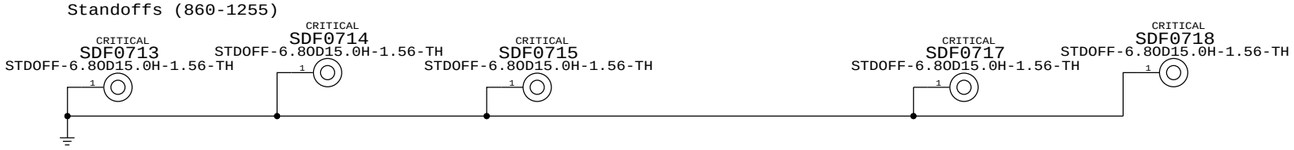
PCH HEATSINK

MOUNTING ANCHORS (511-0057)



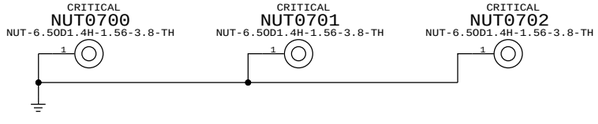
Rear Cover

Standoffs (860-1255)



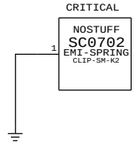
Backer Plate

Nuts (835-0269)



For EMC

EMC Spring (870-1577); Near DIMMs



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 7 OF 110

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UNUSED CPU SIGNALS

TP_CPU_RSVD<41..29>	=	NC_CPU_RSVD<41..29>
TP_CPU_RSVD<26..1>	=	NC_CPU_RSVD<26..1>
TP_CPU_FC_AE38	=	NC_CPU_FC_AE38
TP_CPU_FC_AG40	=	NC_CPU_FC_AG40

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

TP_PCI_AD<31..0>	=	NC_PCI_AD<31..0>
TP_PCI_C_BE_L<3..0>	=	NC_PCI_C_BE_L<3..0>
TP_PCI_PAR	=	NC_PCI_PAR
TP_PCI_RESET_L	=	NC_PCI_RESET_L
TP_PCIE_CLK100M_XDPP	=	NC_PCIE_CLK100M_XDPP
TP_PCIE_CLK100M_XDPN	=	NC_PCIE_CLK100M_XDPN
TP_DMI_CLK100M_LAP	=	NC_DMI_CLK100M_LAP
TP_DMI_CLK100M_LAN	=	NC_DMI_CLK100M_LAN
TP_LPC_DREQ1_L	=	NC_LPC_DREQ1_L
TP_LPC_DREQ0_L	=	NC_LPC_DREQ0_L

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

TP_NV_CE_L<3..0>	=	NC_NV_CE_L<3..0>
TP_NV_DQS<1..0>	=	NC_NV_DQS<1..0>
TP_NV_DQ<15..0>	=	NC_NV_DQ<15..0>
TP_NV_RCOMP	=	NC_NV_RCOMP
TP_NV_RB_L	=	NC_NV_RB_L
TP_NV_WR_RE_L<1..0>	=	NC_NV_WR_RE_L<1..0>
TP_NV_WE_CK_L<1..0>	=	NC_NV_WE_CK_L<1..0>
TP_NV_ALE	=	NC_NV_ALE
TP_NV_CLE	=	NC_NV_CLE

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

TP_MEM_A_CS_L<7..4>	=	NC_MEM_A_CS_L<7..4>
TP_MEM_A_DQ_CB<7..0>	=	NC_MEM_A_DQ_CB<7..0>
TP_MEM_A_DQS_N<8>	=	NC_MEM_A_DQSN<8>
TP_MEM_A_DQS_P<8>	=	NC_MEM_A_DQSP<8>
TP_MEM_B_CS_L<7..4>	=	NC_MEM_B_CS_L<7..4>
TP_MEM_B_DQ_CB<7..0>	=	NC_MEM_B_DQ_CB<7..0>
TP_MEM_B_DQS_N<8>	=	NC_MEM_B_DQSN<8>
TP_MEM_B_DQS_P<8>	=	NC_MEM_B_DQSP<8>

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

TP_HDA_SDIN1	=	NC_HDA_SDIN1
TP_HDA_SDIN2	=	NC_HDA_SDIN2
TP_HDA_SDIN3	=	NC_HDA_SDIN3
TP_JTAG_XDP_TRST_L	=	NC_JTAG_XDP_TRST_L
TP_PCH_PWM0	=	NC_PCH_PWM0
TP_PCH_PWM1	=	NC_PCH_PWM1
TP_PCH_PWM2	=	NC_PCH_PWM2
TP_PCH_PWM3	=	NC_PCH_PWM3
TP_PCH_SST	=	NC_PCH_SST
SNS_CPU_THERMD_N	=	NC_SNS_CPU_THERMDN
SNS_CPU_THERMD_P	=	NC_SNS_CPU_THERMDP

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

TP_PCIE_T28_D2R_N<3..0>	=	NC_PCIE_T28_D2RN<3..0>
TP_PCIE_T28_D2R_P<3..0>	=	NC_PCIE_T28_D2RP<3..0>
TP_PCIE_T28_R2D_C_N<3..0>	=	NC_PCIE_T28_R2D_CN<3..0>
TP_PCIE_T28_R2D_C_P<3..0>	=	NC_PCIE_T28_R2D_CP<3..0>
TP_PCIE_CLK100M_T28_N	=	NC_PCIE_CLK100M_T28N
TP_PCIE_CLK100M_T28_P	=	NC_PCIE_CLK100M_T28P
PCIE_EXCARD_D2R_P	=	NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_D2R_N	=	NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_R2D_C_P	=	NC_PCIE_EXCARD_R2D_CP
PCIE_EXCARD_R2D_C_N	=	NC_PCIE_EXCARD_R2D_CN
PCIE_CLK100M_EXCARD_P	=	NC_PCIE_CLK100M_EXCARDP
PCIE_CLK100M_EXCARD_N	=	NC_PCIE_CLK100M_EXCARDN
TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P
TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N
DMI_MIDBUS_CLK100M_P	=	NC_DMI_MIDBUS_CLK100MP
DMI_MIDBUS_CLK100M_N	=	NC_DMI_MIDBUS_CLK100MN

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

TP_USB_1N	=	NC_USB_1N
TP_USB_1P	=	NC_USB_1P
TP_USB_2N	=	NC_USB_2N
TP_USB_2P	=	NC_USB_2P
TP_USB_3N	=	NC_USB_3N
TP_USB_3P	=	NC_USB_3P
TP_USB_4N	=	NC_USB_4N
TP_USB_4P	=	NC_USB_4P
TP_USB_5N	=	NC_USB_5N
TP_USB_5P	=	NC_USB_5P
TP_USB_6N	=	NC_USB_6N
TP_USB_6P	=	NC_USB_6P
TP_USB_7N	=	NC_USB_7N
TP_USB_7P	=	NC_USB_7P
TP_USB_9N	=	NC_USB_9N
TP_USB_9P	=	NC_USB_9P
TP_USB_10N	=	NC_USB_10N
TP_USB_10P	=	NC_USB_10P
TP_USB_11N	=	NC_USB_11N
TP_USB_11P	=	NC_USB_11P
TP_USB_12N	=	NC_USB_12N
TP_USB_12P	=	NC_USB_12P
TP_USB_13N	=	NC_USB_13N
TP_USB_13P	=	NC_USB_13P

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

TP_CRT_IG_DDC_CLK	=	NC_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA	=	NC_CRT_IG_DDC_DATA
TP_CRT_IG_RED	=	NC_CRT_IG_RED
TP_CRT_IG_GREEN	=	NC_CRT_IG_GREEN
TP_CRT_IG_BLUE	=	NC_CRT_IG_BLUE
TP_CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC
TP_CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC
TP_DP_IG_B_MLN<3..0>	=	NC_DP_IG_B_MLN<3..0>
TP_DP_IG_B_MLP<3..0>	=	NC_DP_IG_B_MLP<3..0>
TP_DP_IG_B_AUX_N	=	NC_DP_IG_B_AUXN
TP_DP_IG_B_AUX_P	=	NC_DP_IG_B_AUXP
TP_DP_IG_B_HPD	=	NC_DP_IG_B_HPD
TP_DP_IG_B_DDC_CLK	=	NC_DP_IG_B_CTRL_CLK
TP_DP_IG_B_DDC_DATA	=	NC_DP_IG_B_CTRL_DATA
TP_DP_IG_C_MLN<3..0>	=	NC_DP_IG_C_MLN<3..0>
TP_DP_IG_C_MLP<3..0>	=	NC_DP_IG_C_MLP<3..0>
TP_DP_IG_C_AUX_N	=	NC_DP_IG_C_AUXN
TP_DP_IG_C_AUX_P	=	NC_DP_IG_C_AUXP
TP_DP_IG_C_HPD	=	NC_DP_IG_C_HPD
TP_DP_IG_C_CTRL_CLK	=	NC_DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA	=	NC_DP_IG_C_CTRL_DATA
TP_DP_IG_D_MLN<3..0>	=	NC_DP_IG_D_MLN<3..0>
TP_DP_IG_D_MLP<3..0>	=	NC_DP_IG_D_MLP<3..0>
TP_DP_IG_D_AUXN	=	NC_DP_IG_D_AUXN
TP_DP_IG_D_AUXP	=	NC_DP_IG_D_AUXP
TP_DP_IG_D_HPD	=	NC_DP_IG_D_HPD
TP_DP_IG_D_CTRL_CLK	=	NC_DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA	=	NC_DP_IG_D_CTRL_DATA
TP_GFX_VID<0..6>	=	NC_GFX_VID<0..6>
TP_GFX_VSENSE_N	=	NC_GFX_VSENSEN
TP_GFX_VSENSE_P	=	NC_GFX_VSENSEP
TP_SDVO_TVCLKINN	=	NC_SDVO_TVCLKINN
TP_SDVO_TVCLKINP	=	NC_SDVO_TVCLKINP
TP_SDVO_STALLN	=	NC_SDVO_STALLN
TP_SDVO_STALLP	=	NC_SDVO_STALLP
TP_SDVO_INTN	=	NC_SDVO_INTN
TP_SDVO_INTP	=	NC_SDVO_INTP

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

TP_CPU_FDI_TX_N<7..0>	=	NC_CPU_FDI_TXN<7..0>
TP_CPU_FDI_TX_P<7..0>	=	NC_CPU_FDI_TXP<7..0>
TP_PCH_FDI_RX_N<7..0>	=	NC_PCH_FDI_RXN<7..0>
TP_PCH_FDI_RX_P<7..0>	=	NC_PCH_FDI_RXP<7..0>
TP_CPU_FDI_FSYNC<1..0>	=	NC_CPU_FDI_FSYNC<1..0>
TP_PCH_FDI_FSYNC<1..0>	=	NC_PCH_FDI_FSYNC<1..0>
TP_CPU_FDI_LSYNC<1..0>	=	NC_CPU_FDI_LSYNC<1..0>
TP_PCH_FDI_LSYNC<1..0>	=	NC_PCH_FDI_LSYNC<1..0>
TP_CPU_FDI_INT	=	NC_CPU_FDI_INT
TP_PCH_FDI_INT	=	NC_PCH_FDI_INT

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

TP_SATA_D_D2RN	=	NC_SATA_D_D2RN
TP_SATA_D_D2RP	=	NC_SATA_D_D2RP
TP_SATA_D_R2D_CN	=	NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP	=	NC_SATA_D_R2D_CP
TP_SATA_E_D2RN	=	NC_SATA_E_D2RN
TP_SATA_E_D2RP	=	NC_SATA_E_D2RP
TP_SATA_E_R2D_CN	=	NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP	=	NC_SATA_E_R2D_CP
TP_SATA_F_D2RN	=	NC_SATA_F_D2RN
TP_SATA_F_D2RP	=	NC_SATA_F_D2RP
TP_SATA_F_R2D_CN	=	NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP	=	NC_SATA_F_R2D_CP
TP_SATA_SSD_D2R_N	=	NC_SATA_SSD_D2RN
TP_SATA_SSD_D2R_P	=	NC_SATA_SSD_D2RP
TP_SATA_SSD_R2D_C_N	=	NC_SATA_SSD_R2D_CN
TP_SATA_SSD_R2D_C_P	=	NC_SATA_SSD_R2D_CP

MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

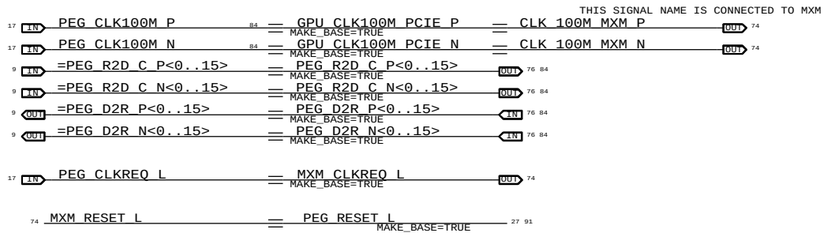
REVISION: A.0.0

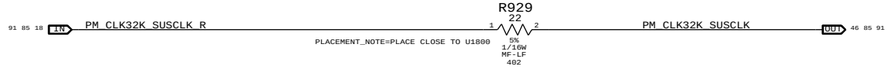
BRANCH:

PAGE: 8 OF 110

SHEET: 7 OF 92

PEG Slot Support





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PAGE TITLE: Signal Aliases

Apple Inc.

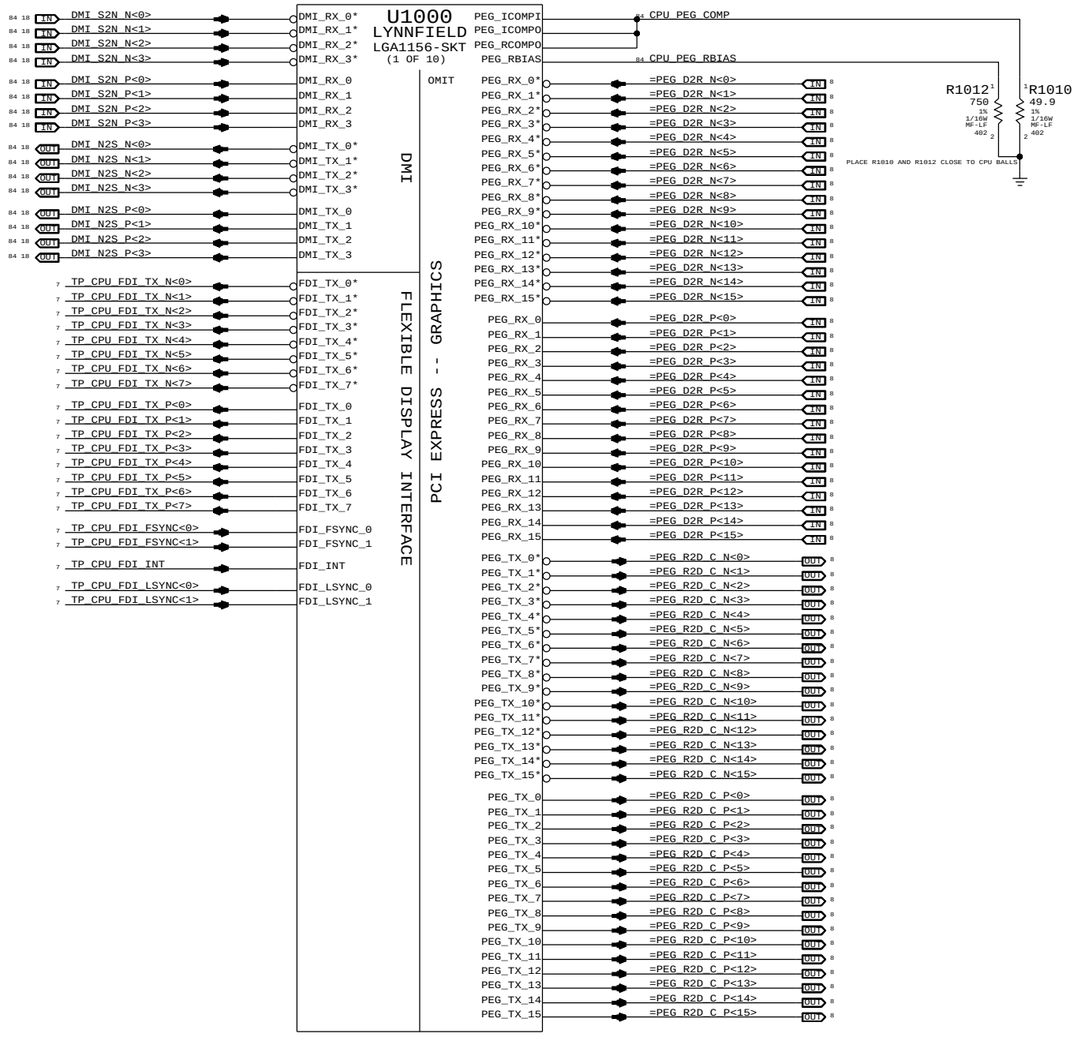
DRAWING NUMBER: 051-8337 SIZE: D

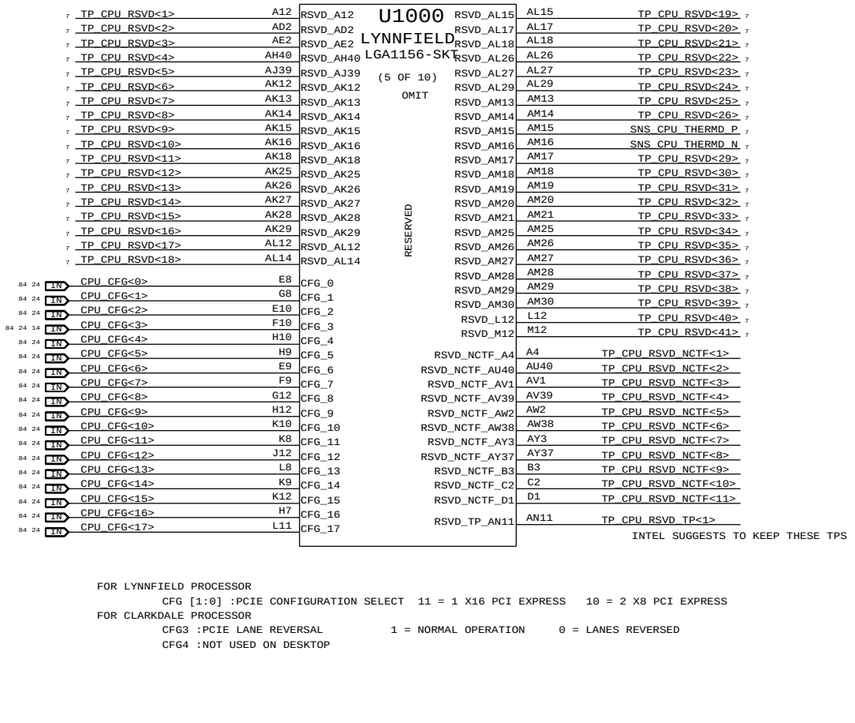
REVISION: A.0.0

BRANCH:

PAGE: 9 OF 110

SHEET: 8 OF 92





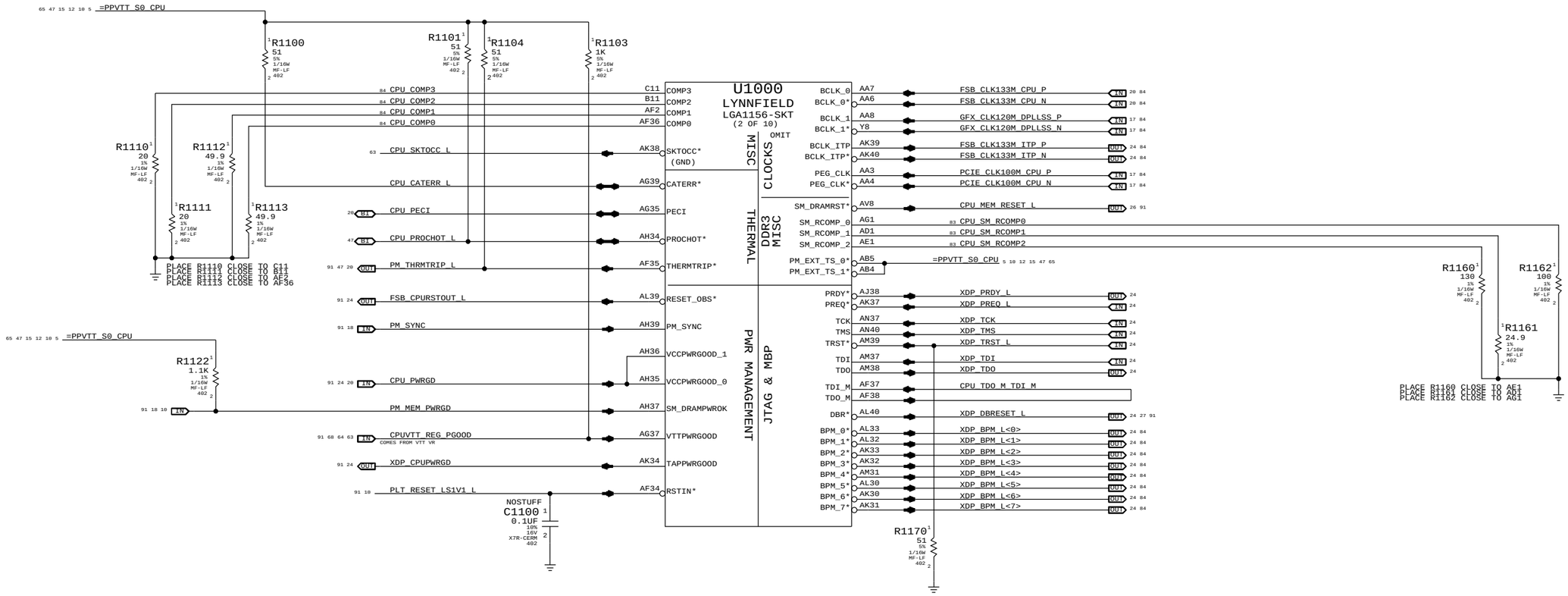
FOR LYNNFIELD PROCESSOR
CFG [1:0] :PCIE CONFIGURATION SELECT 11 = 1 X16 PCI EXPRESS 10 = 2 X8 PCI EXPRESS
FOR CLARKDALE PROCESSOR
CFG3 :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG4 :NOT USED ON DESKTOP

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

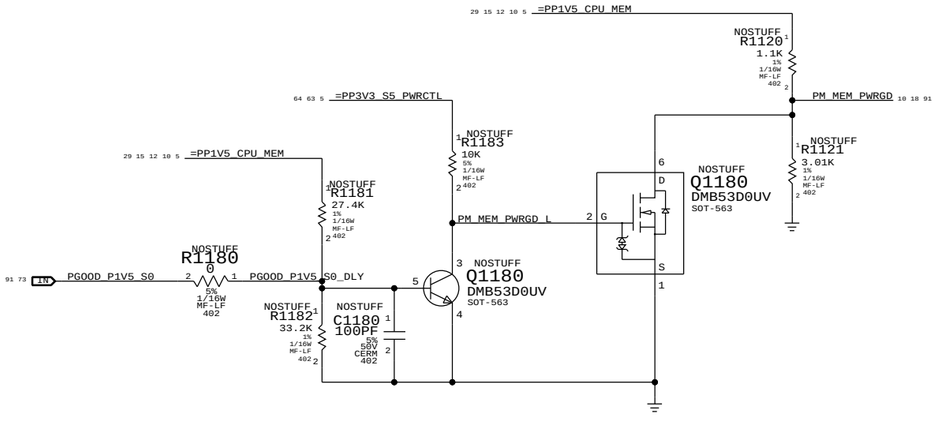
Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
PAGE 10 OF 110
SHEET 9 OF 92

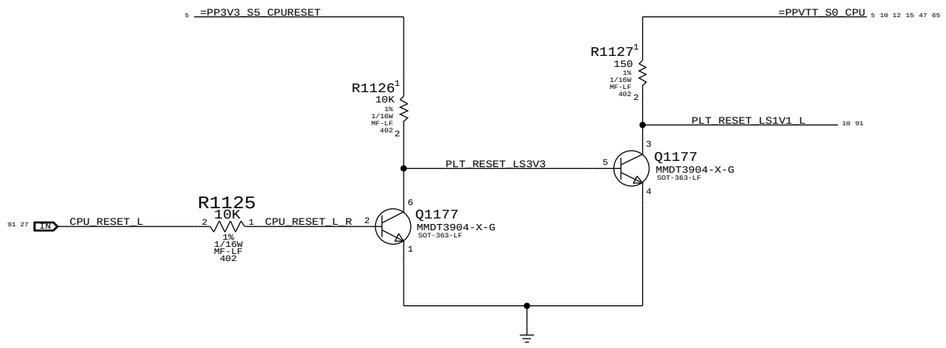


PM_MEM_PWRGD MUST ASSERT MIN. 100 NS AFTER =PP1V5_CPU_MEM IS STABLE
PRIMARY SOLUTION: PULL PM_MEM_PWRGD TO CPU VTT, WHICH RISES SEVERAL MS AFTER 1.5V. STUFF R1122

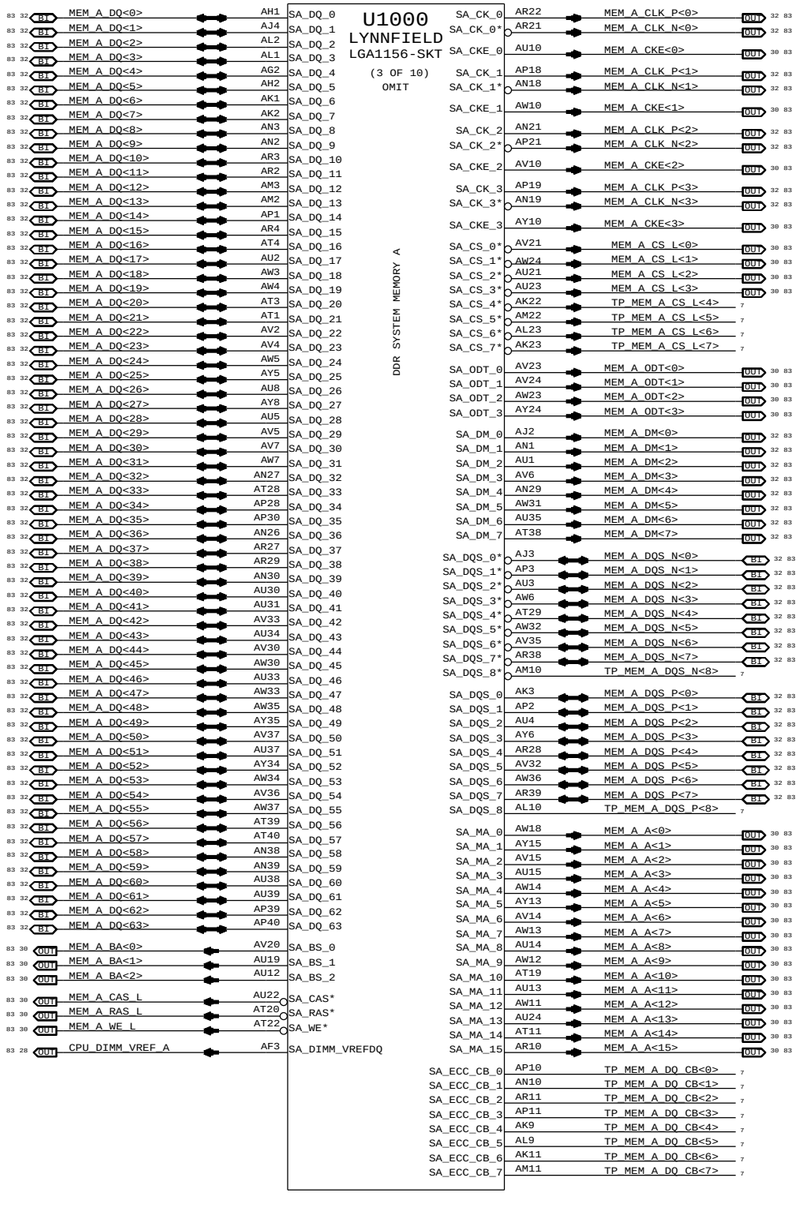
BACKUP SOLUTION (FOR CLEANER EDGE): PULL TO 1.5V (DIVIDED) AND DELAY PGOOD. NO-STUFF R1122, STUFF CIRCUIT BELOW
R1180-R1182 PROVIDE OPTIONS TO TRIGGER FROM RISE OF 1.5V, OR FROM PGOOD
C1180 CAN BE TUNED FOR SPECIFIC DELAY

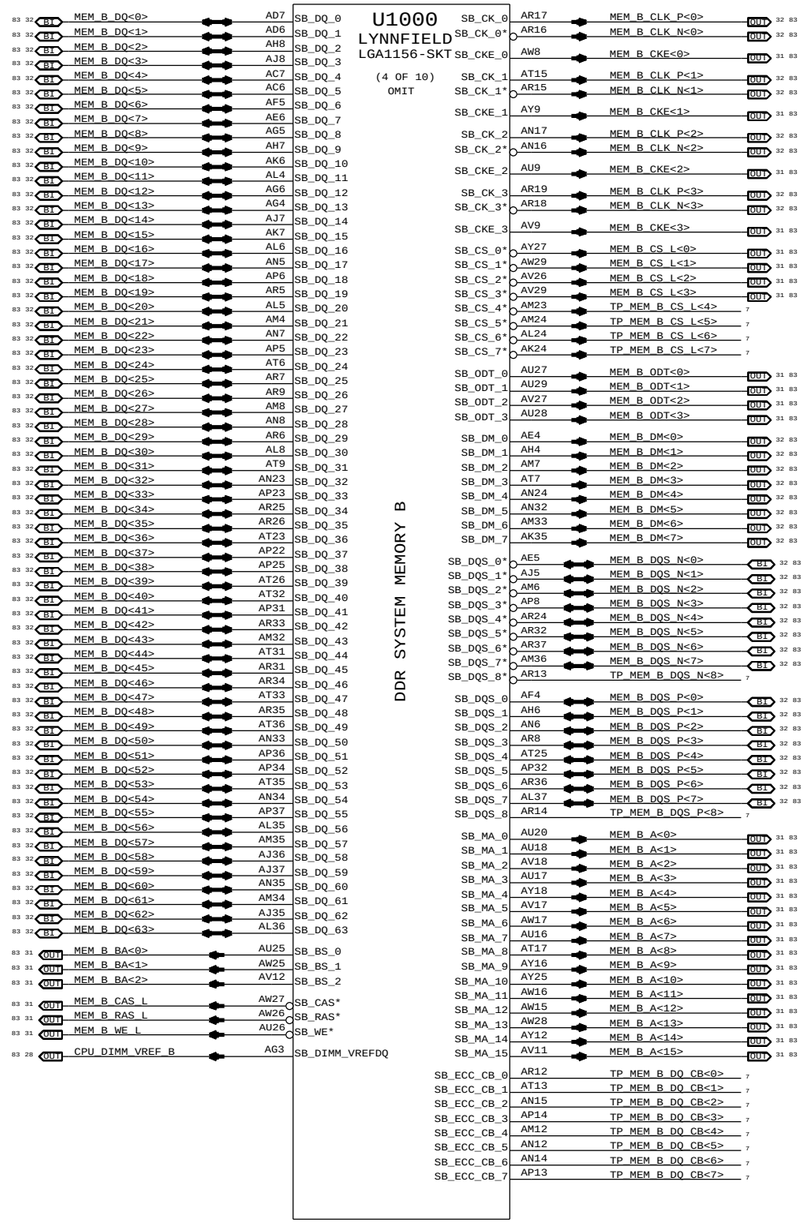


CPU RESET LEVEL SHIFTER



SYNC_MASTER=K74_MASTER	SYNC_DATE=N/A
PAGE TITLE: CPU CLOCK/MISC/JTAG	
Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 11 OF 110
	SHEET: 10 OF 92





SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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=PPVCORE_S0_CPU 5 12 15

U1000
LYNNFIELD
LGA1156-SKT
(10 OF 10)
OMIT

VCC

J21	VCC_100	
J22	VCC_101	
J24	VCC_102	
J25	VCC_103	
J27	VCC_104	
J28	VCC_105	
J30	VCC_106	
J31	VCC_107	
J33	VCC_108	
J34	VCC_109	
J36	VCC_110	
J37	VCC_111	
J39	VCC_112	
J40	VCC_113	
K17	VCC_114	
K18	VCC_115	
K20	VCC_116	
K21	VCC_117	
K23	VCC_118	
K24	VCC_119	
K26	VCC_120	
K27	VCC_121	
K29	VCC_122	
K30	VCC_123	
K32	VCC_124	
K33	VCC_125	
K35	VCC_126	
K36	VCC_127	
K38	VCC_128	
K39	VCC_129	
L17	VCC_130	
L19	VCC_131	
L20	VCC_132	
L22	VCC_133	
L23	VCC_134	
L25	VCC_135	
L26	VCC_136	
L28	VCC_137	
L29	VCC_138	
L31	VCC_139	
L32	VCC_140	
L34	VCC_141	
L35	VCC_142	
L37	VCC_143	
L38	VCC_144	
L40	VCC_145	
M17	VCC_146	
M19	VCC_147	
M21	VCC_148	
M22	VCC_149	
M24	VCC_150	
M25	VCC_151	
M27	VCC_152	
M28	VCC_153	
M30	VCC_154	
M33	VCC_155	
M34	VCC_156	
M36	VCC_157	
M37	VCC_158	
M39	VCC_159	
M40	VCC_160	
N33	VCC_161	
N35	VCC_162	
N36	VCC_163	
N38	VCC_164	
N39	VCC_165	
P33	VCC_166	
P34	VCC_167	
P35	VCC_168	
P36	VCC_169	
P37	VCC_170	
P38	VCC_171	
P39	VCC_172	
P40	VCC_173	
R33	VCC_174	
R34	VCC_175	
R35	VCC_176	
R36	VCC_177	
R37	VCC_178	
R38	VCC_179	
R39	VCC_180	
R40	VCC_181	

NCTF

CGC_TP_NCTF	B39	TP_CPU_CGC_NCTF
VCC_NCTF_0	A38	=PPVCORE_S0_CPU 5 12 15
VCC_NCTF_1	C40	
FC_AE38	AE38	TP_CPU_FC_AE38 7
FC_AG40	AG40	TP_CPU_FC_AG40 7

15 12 5 =PPVCORE_S0_CPU

U1000
LYNNFIELD
LGA1156-SKT
(6 OF 10)
OMIT

CPU CORE SUPPLY

A23	VCC_0	
A24	VCC_1	
A26	VCC_2	
A27	VCC_3	
A33	VCC_4	
A35	VCC_5	
A36	VCC_6	
B23	VCC_7	
B25	VCC_8	
B26	VCC_9	
B28	VCC_10	
B29	VCC_11	
B31	VCC_12	
B32	VCC_13	
B34	VCC_14	
B35	VCC_15	
B37	VCC_16	
B38	VCC_17	
C23	VCC_18	
C24	VCC_19	
C25	VCC_20	
C27	VCC_21	
C28	VCC_22	
C30	VCC_23	
C31	VCC_24	
C33	VCC_25	
C34	VCC_26	
C36	VCC_27	
C37	VCC_28	
C39	VCC_29	
D23	VCC_30	
D24	VCC_31	
D26	VCC_32	
D27	VCC_33	
D29	VCC_34	
D30	VCC_35	
D32	VCC_36	
D33	VCC_37	
D35	VCC_38	
D36	VCC_39	
D38	VCC_40	
D39	VCC_41	
E22	VCC_42	
E23	VCC_43	
E25	VCC_44	
E26	VCC_45	
E28	VCC_46	
E29	VCC_47	
E31	VCC_48	
E32	VCC_49	
E34	VCC_50	
E35	VCC_51	
E37	VCC_52	
E38	VCC_53	
E40	VCC_54	
F21	VCC_55	
F22	VCC_56	
F24	VCC_57	
F25	VCC_58	
F27	VCC_59	
F28	VCC_60	
F30	VCC_61	
F31	VCC_62	
F33	VCC_63	
F34	VCC_64	
F36	VCC_65	
F37	VCC_66	
F39	VCC_67	
F40	VCC_68	
G20	VCC_69	
G21	VCC_70	
G23	VCC_71	
G24	VCC_72	
G26	VCC_73	
G27	VCC_74	
G29	VCC_75	
G30	VCC_76	
G32	VCC_77	
G33	VCC_78	
G35	VCC_79	
G36	VCC_80	
G38	VCC_81	
G39	VCC_82	
H19	VCC_83	
H20	VCC_84	
H22	VCC_85	
H23	VCC_86	
H25	VCC_87	
H26	VCC_88	
H28	VCC_89	
H29	VCC_90	
H31	VCC_91	
H32	VCC_92	
H34	VCC_93	
H35	VCC_94	
H37	VCC_95	
H38	VCC_96	
H40	VCC_97	
J18	VCC_98	
J19	VCC_99	

1.1V RAIL POWER

AA33	VTT_0	
AA34	VTT_1	
AA35	VTT_2	
AA36	VTT_3	
AA37	VTT_4	
AA38	VTT_5	
AB7	VTT_6	
AC33	VTT_7	
AC34	VTT_8	
AC35	VTT_9	
AC36	VTT_10	
AC37	VTT_11	
AC38	VTT_12	
AC39	VTT_13	
AC40	VTT_14	
AC5	VTT_15	
AC8	VTT_16	
AD33	VTT_17	
AD34	VTT_18	
AD35	VTT_19	
AD36	VTT_20	
AD37	VTT_21	
AD38	VTT_22	
AD39	VTT_23	
AD40	VTT_24	
AE33	VTT_25	
AE34	VTT_26	
AE39	VTT_27	
AE40	VTT_28	
AE8	VTT_29	
AF33	VTT_30	
AG33	VTT_31	
AJ17	VTT_32	
AJ19	VTT_33	
AJ21	VTT_34	
AJ23	VTT_35	
AJ25	VTT_36	
AJ27	VTT_37	
AJ29	VTT_38	
AJ31	VTT_39	
AJ32	VTT_40	
AK19	VTT_41	
AK20	VTT_42	
AK21	VTT_43	
AL20	VTT_44	
AL21	VTT_45	
L10	VTT_46	
M10	VTT_47	
M11	VTT_48	
M9	VTT_49	
N7	VTT_50	
P6	VTT_51	
P7	VTT_52	
P8	VTT_53	
T2	VTT_54	
T6	VTT_55	
T7	VTT_56	
T8	VTT_57	
V2	VTT_58	
V33	VTT_59	
V34	VTT_60	
V35	VTT_61	
V36	VTT_62	
V37	VTT_63	
V38	VTT_64	
V39	VTT_65	
V40	VTT_66	
V6	VTT_67	
V7	VTT_68	
V8	VTT_69	
W1	VTT_70	
W6	VTT_71	
Y33	VTT_72	
Y34	VTT_73	
Y35	VTT_74	
Y36	VTT_75	
Y37	VTT_76	
Y38	VTT_77	

CPU VIDS

PSI*	AG38	CPU_PSI_L	OUT 65 89
VID_0/MSID_0	U40	CPU_VID<0>	OUT 15 65 89
VID_1/MSID_1	U39	CPU_VID<1>	OUT 15 65 89
VID_2/MSID_2	U38	CPU_VID<2>	OUT 15 65 89
VID_3/CSC_0	U37	CPU_VID<3>	OUT 15 65 89
VID_4/CSC_1	U36	CPU_VID<4>	OUT 15 65 89
VID_5/CSC_2	U35	CPU_VID<5>	OUT 15 65 89
VID_6	U34	CPU_VID<6>	OUT 15 65 89
VID_7	U33	CPU_VID<7>	OUT 15 65 89
VTT_SELECT	AF39	TP_CPU_VTTSELECT	

SENSE LINES

ISENSE	T40	VR_CPU_IOUT	CONNECTED TO THE IMON OUT FROM CPU REG IN 65 88
VCC_SENSE	T35	CPU_VCC_PKG_SENSE_P	OUT 50 65 89
VSS_SENSE	T34	CPU_VCC_PKG_SENSE_N	OUT 65 89
VTT_SENSE	AE35	CPU_VTTSENSE_P	OUT 68 89
VSS_SENSE_VTT	AE36	CPU_VTTSENSE_N	OUT 68 89

POWER

5 =PPVAXG_S0_CPU
THIS SUPPLY IS NEEDED ONLY FOR SYSTEM WITH DALE IG

U1000
LYNNFIELD
LGA1156-SKT
(7 OF 10)
OMIT

GRAPHICS

A14	VAXG_0
A15	VAXG_1
A17	VAXG_2
A18	VAXG_3
B14	VAXG_4
B15	VAXG_5
B17	VAXG_6
B18	VAXG_7
C14	VAXG_8
C15	VAXG_9
C17	VAXG_10
C18	VAXG_11
C20	VAXG_12
C21	VAXG_13
D14	VAXG_14
D15	VAXG_15
D17	VAXG_16
D18	VAXG_17
D20	VAXG_18
D21	VAXG_19
E14	VAXG_20
E15	VAXG_21
E17	VAXG_22
E18	VAXG_23
E20	VAXG_24
F14	VAXG_25
F15	VAXG_26
F17	VAXG_27
F18	VAXG_28
F19	VAXG_29
G14	VAXG_30
G15	VAXG_31
G17	VAXG_32
G18	VAXG_33
H14	VAXG_34
H15	VAXG_35
H17	VAXG_36
J14	VAXG_37
J15	VAXG_38
J16	VAXG_39
K14	VAXG_40
K15	VAXG_41
K16	VAXG_42
L14	VAXG_43
L15	VAXG_44
L16	VAXG_45
M14	VAXG_46
M15	VAXG_47
M16	VAXG_48

SENSE LINES

VSSAXG_SENSE	B13	TP_GFX_VSENSE_N 7
VAXG_SENSE	A13	TP_GFX_VSENSE_P 7

GRAPHICS VIDS

GFX_VID_0	G10	TP_GFX_VID<0> 7
GFX_VID_1	B12	TP_GFX_VID<1> 7
GFX_VID_2	E12	TP_GFX_VID<2> 7
GFX_VID_3	E11	TP_GFX_VID<3> 7
GFX_VID_4	C12	TP_GFX_VID<4> 7
GFX_VID_5	G11	TP_GFX_VID<5> 7
GFX_VID_6	J11	TP_GFX_VID<6> 7
GFX_VR_EN	F12	TP_GFX_VR_EN
GFX_DPRSLPVR	J10	TP_GFX_DPRSLPVR
GFX_IMON	F6	

=PP1V5_CPU_MEM 5 10 15 29

POWER

DDR3-1.5V RAILS

VDDQ_0	AJ11	
VDDQ_1	AJ13	
VDDQ_2	AJ15	
VDDQ_3	AT10	
VDDQ_4	AT18	
VDDQ_5	AT21	
VDDQ_6	AU11	
VDDQ_7	AV13	
VDDQ_8	AV16	
VDDQ_9	AV19	
VDDQ_10	AV22	
VDDQ_11	AV25	
VDDQ_12	AV28	
VDDQ_13	AW9	
VDDQ_14	AY11	
VDDQ_15	AY14	
VDDQ_16	AY17	
VDDQ_17	AY23	
VDDQ_18	AY26	

=PP1V8_S0_CPU_PLL 5 15 64

1.8V

VCCPLL_0	AF7	
VCCPLL_1	AF8	
VCCPLL_2	AG8	

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU POWER

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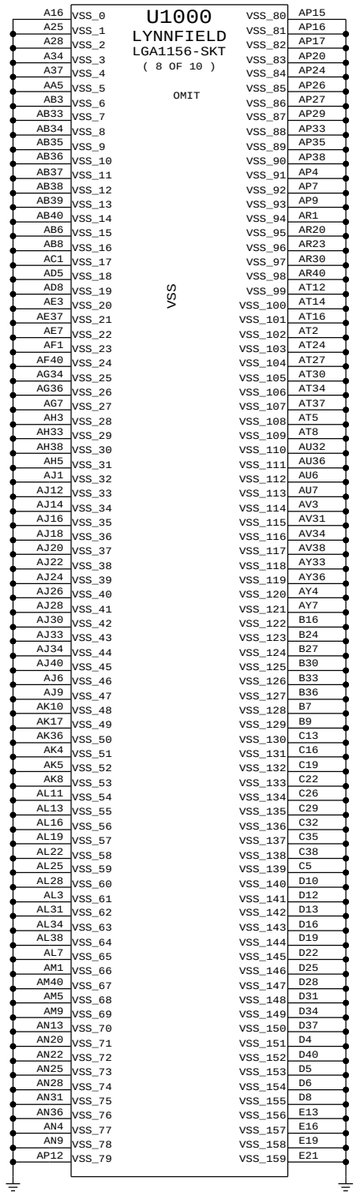

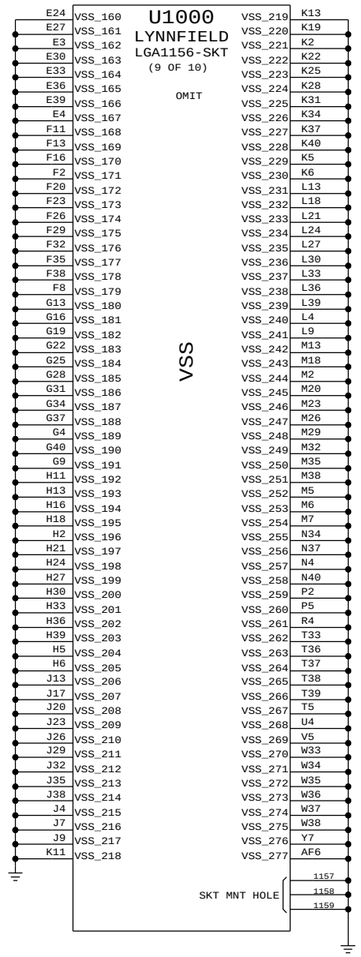

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

CPU GROUNDS

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84 24 9 CPU_CFG<3>

R1500 1.5K 5% 1/16W MF-LF 402

CPU_CFG<3> IS USED FOR PCIE LANE REVERSAL

CPU_CFG<3>	PCIE LANES
0	REVERSAL
1	NO REVERSAL

UNUSED GPIO SIGNALS

14 5 =PP3V3_S0_PCH_STRAPS

R1591 10K 5% 1/16W MF-LF 402
R1529 10K 5% 1/16W MF-LF 402
R1523 10K 5% 1/16W MF-LF 402
R1524 10K 5% 1/16W MF-LF 402
R1528 10K 5% 1/16W MF-LF 402
R1508 10K 5% 1/16W MF-LF 402
R1526 10K 5% 1/16W MF-LF 402
R1504 10K 5% 1/16W MF-LF 402
R1506 10K 5% 1/16W MF-LF 402
R1503 10K 5% 1/16W MF-LF 402
R1509 10K 5% 1/16W MF-LF 402

PCH_GPIO0_BMBUSY_L 20
PCH_GPIO21_SATA0GP 17
PCH_GPIO19_SATA1GP 17
PCH_GPIO37_SATA3GP 20
PCH_GPIO49_SATA5GP 20
PCH_GPIO6_TACH2 20
PCH_GPIO34_STP_PCI_L 20
PCH_GPIO38_SLOAD 20
PCH_GPIO39_SDATAOUT0 20
AP_PWR_EN 20
FW_PWR_EN 20

UNUSED GPIO SIGNALS

14 5 =PP3V3_S5_PCH_STRAPS

R1538 10K 5% 1/16W MF-LF 402
R1535 10K 5% 1/16W MF-LF 402
R1590 10K 5% 1/16W MF-LF 402
BUF_CLK R1517 10K 5% 1/16W MF-LF 402

PCH_GPIO8_FCIM_EN_L 20
PCH_GPIO24 20
BRCRYPT_PWR_EN 17
PCH_GPIO15 20

37 17 ENET_ENERGY_DET
37 20 ENET_LOW_PWR
91 18 PM_LAN_PWRGD

R1501 10K 5% 1/16W MF-LF 402
R1510 10K 5% 1/16W MF-LF 402
R1511 10K 5% 1/16W MF-LF 402

14 5 =PP3V3_S0_PCH_STRAPS

R1525 10K 5% 1/16W MF-LF 402
R1522 10K 5% 1/16W MF-LF 402
R1539 10K 5% 1/16W MF-LF 402

ENET_CLKREQ_L 17 37
FW_CLKREQ_L 17 40
MINI_CLKREQ_L 17 33

14 5 =PP3V3_S5_PCH_STRAPS

PCH_VRM R1530 10K 5% 1/16W MF-LF 402
R1515 10K 5% 1/16W MF-LF 402

PM_BATLOW_L 18 45 91
PCH_GPIO27_VRMEN 20

14 5 =PP3V3_S0_PCH_STRAPS

R1575 10K 5% 1/16W MF-LF 402
R1574 10K 5% 1/16W MF-LF 402
R1573 10K 5% 1/16W MF-LF 402
R1571 10K 5% 1/16W MF-LF 402
R1570 10K 5% 1/16W MF-LF 402
R1543 10K 5% 1/16W MF-LF 402

PCH_SPKR 17
PM_CLKRUN_L 18 46 48 91
SPI_DESCRIPTOR_OVERRIDE_L 17 46
BRCRYPT_RESET 17
PCH_CLKOUTFLEX1 17
PCH_CLKOUTFLEX2 17
PCH_CLKOUTFLEX3 17

R1572 10K 5% 1/16W MF-LF 402

UNUSED CLKREQS

14 5 =PP3V3_S0_PCH_STRAPS

R1536 10K 5% 1/16W MF-LF 402
R1532 10K 5% 1/16W MF-LF 402
R1533 10K 5% 1/16W MF-LF 402

EXCARD_CLKREQ_L 17
T28_CLKREQ_L 17
PEB_CLKREQ_L 17

NOSTUFF R1537 10K 5% 1/16W MF-LF 402

IF LIKE TO HAVE THE PEB CLOCKS ENABLED. STUFF R1535 AND UNSTUFF R1534

14 5 =PP3V3_S0_PCH_STRAPS

R1527 10K 5% 1/16W MF-LF 402
R1507 10K 5% 1/16W MF-LF 402

FW_PME_L 20 40
SMC_RUNTIME_SCI_L 20 46

20 ODD_PWR_EN_L
36 20 WOL_EN
20 PCH_INIT3V3_L

NOSTUFF R1550 1K 5% 1/16W MF-LF 402
R1555 10K 5% 1/16W MF-LF 402
R1512 10K 5% 1/16W MF-LF 402

BOOT STRAP OPTIONS

19 PCH_PCI_GNT3_L
19 PCH_PCI_GNT2_L
19 PCH_PCI_GNT1_L
19 PCH_PCI_GNT0_L

NOSTUFF R1551 10K 5% 1/16W MF-LF 402
NOSTUFF R1552 10K 5% 1/16W MF-LF 402
NOSTUFF R1553 10K 5% 1/16W MF-LF 402
NOSTUFF R1554 10K 5% 1/16W MF-LF 402

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

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CPU VCORE DECOUPLING

INTEL RECOMMENDATION 17X 22UF 0805

12 5 =PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609
C1610 C1611 C1612 C1613 C1614 C1615 C1616 NOSTUFF C1617 NOSTUFF C1618 NOSTUFF C1619

22UF 20% 6.3V CERM-X5R 805-3

BULK CAPS ON CPU VREG PAGE 74

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

65 47 15 12 10 5 =PPVTT_S0_CPU

CPUMSI0U R1600 1K 5% 1/16W MF-LF 402
CPUMSI2U R1602 1K 5% 1/16W MF-LF 402
CPUPOC4U R1604 1K 5% 1/16W MF-LF 402
CPUMSI1U R1601 1K 5% 1/16W MF-LF 402
CPUPOC3U R1603 1K 5% 1/16W MF-LF 402
CPUPOC5U R1605 1K 5% 1/16W MF-LF 402

89 65 12 OUT CPU_VID<0>
89 65 12 OUT CPU_VID<1>
89 65 12 OUT CPU_VID<2>
89 65 12 OUT CPU_VID<3>
89 65 12 OUT CPU_VID<4>
89 65 12 OUT CPU_VID<5>
89 65 12 OUT CPU_VID<6>
89 65 12 OUT CPU_VID<7>

CPUMSI0D R1610 1K 5% 1/16W MF-LF 402
CPUMSI2D R1612 1K 5% 1/16W MF-LF 402
CPUPOC4D R1614 1K 5% 1/16W MF-LF 402
R1616 1K 5% 1/16W MF-LF 402
CPUMSI1D R1611 1K 5% 1/16W MF-LF 402
CPUPOC3D R1613 1K 5% 1/16W MF-LF 402
CPUPOC5D R1615 1K 5% 1/16W MF-LF 402
R1617 1K 5% 1/16W MF-LF 402

VID[2:0] = FUNCTION MSI[2:0]
VID[5:3] = IMON CONFIG DEFAULT
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)

VTT (CPU Uncore) DECOUPLING

8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805

65 47 15 12 10 5 =PPVTT_S0_CPU

PLACEMENT_NOTE (C1650-C1657):
Place under socket cavity on secondary side.

C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657

22UF 20% 6.3V CERM-X5R 805

PLACEMENT_NOTE (C1660-C1666):
Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660 C1661 C1662 C1663 C1664 C1665 C1666

10uF 20% 6.3V X5R 603

BULK CAPS ON CPU VTT REG PAGE 74

C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C1671 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402

29 12 10 5 =PP1V5_CPU_MEM

C1680 22uF 20% 6.3V CERM-X5R 805
C1681 22uF 20% 6.3V CERM-X5R 805
C1682 1UF 10% 10V X5R 402
C1683 1UF 10% 10V X5R 402
C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402

PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402

64 12 5 =PP1V8_S0_CPU_PLL

C1690 22uF 20% 6.3V CERM-X5R 805
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1692 2.2UF 10% 6.3V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402

MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC5D,CPUPOC4D,CPUPOC3D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC5D,CPUPOC4D,CPUPOC3U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC5D,CPUPOC4U,CPUPOC3D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC5D,CPUPOC4U,CPUPOC3U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC5U,CPUPOC4D,CPUPOC3D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC5U,CPUPOC4D,CPUPOC3U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC5U,CPUPOC4U,CPUPOC3D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC5U,CPUPOC4U,CPUPOC3U	10

BOM GROUP	BOM OPTIONS
CLARKDALE_73W	CKD,CPUPOC_IMAX_60_80,CPUMSI2U,CPUMSI1D,CPUMSI0U
LYNNFIELD_82W	LFD,CPUPOC_IMAX_60_80,CPUMSI2U,CPUMSI1D,CPUMSI0U
LYNNFIELD_95W	LFD,CPUPOC_IMAX_100_120,CPUMSI2U,CPUMSI1U,CPUMSI0D

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
CPU NON-GFX DECOUPLING

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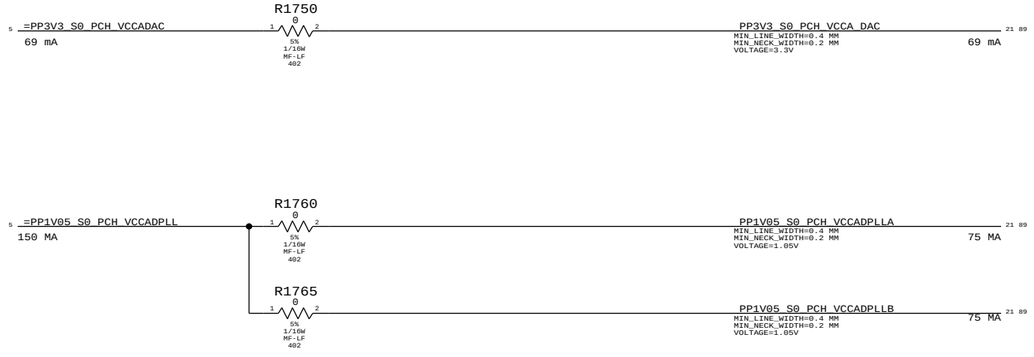

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU/PCH GFX DECOUPLING

Apple Inc.

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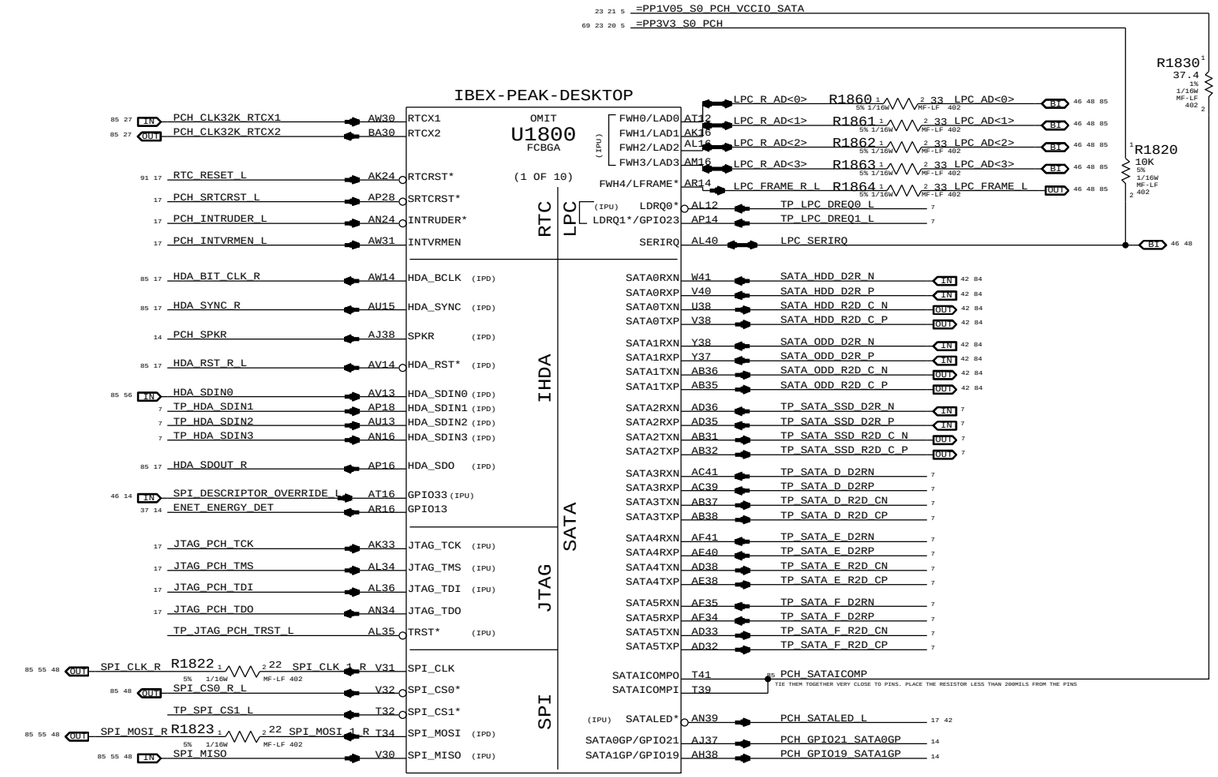

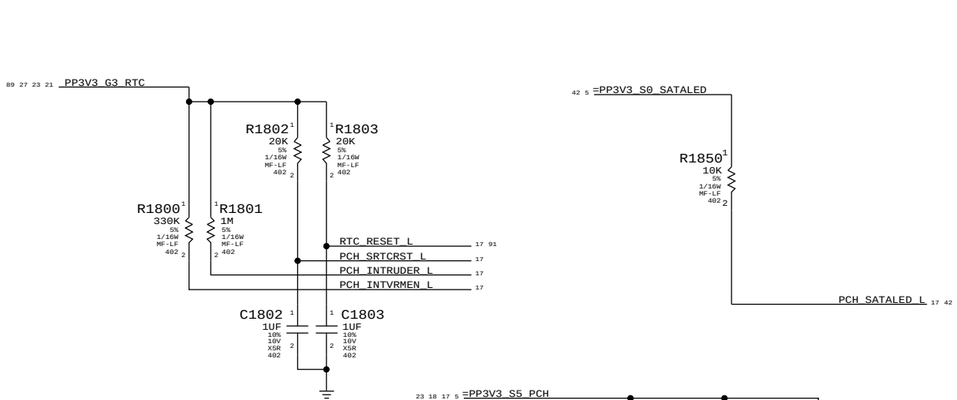

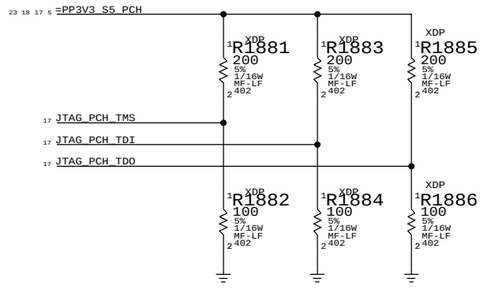

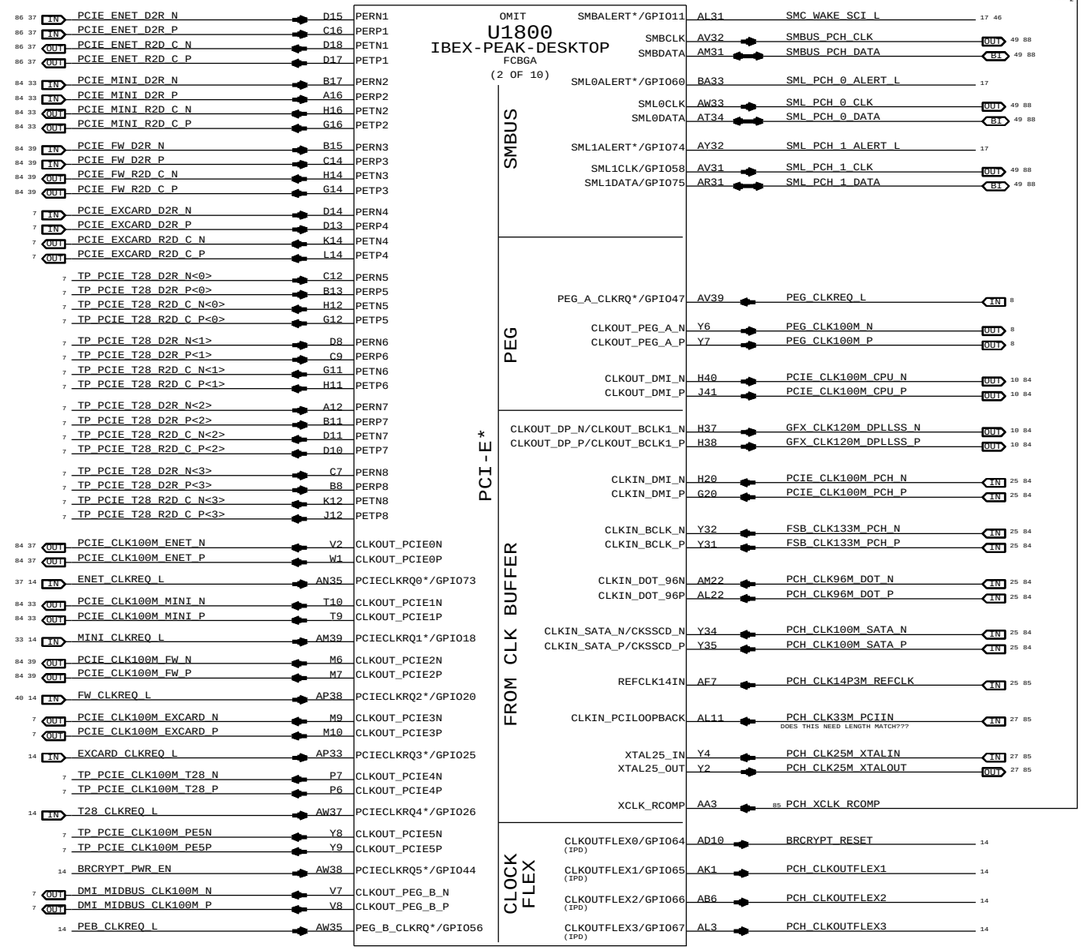

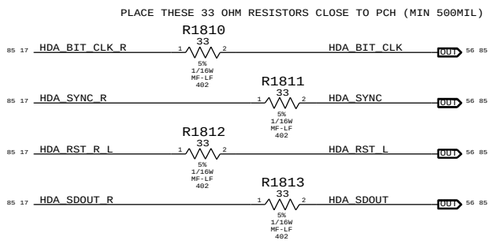

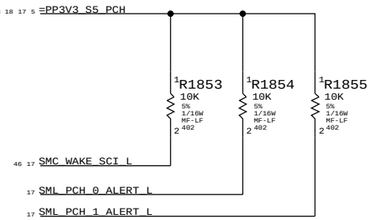

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

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=PP3V3_S5_PCH 5 17 18 23
=PP1V05_S0_PCH_VCCIO_PCIE 5 17 21 23

R1905 10K 1% 1/16W MF-LF 402
R1915 100K 1% 1/16W MF-LF 402
R1900 49.9 1% 1/16W MF-LF 402

IBEX-PEAK-DESKTOP

OMIT
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DMI

84 9 IN DMI_N2S_N<0>	A19	DMI0RXN	
84 9 IN DMI_N2S_N<1>	B20	DMI1RXN	
84 9 IN DMI_N2S_N<2>	E20	DMI2RXN	
84 9 IN DMI_N2S_N<3>	G18	DMI3RXN	
84 9 IN DMI_N2S_P<0>	B18	DMI0RXP	
84 9 IN DMI_N2S_P<1>	C19	DMI1RXP	
84 9 IN DMI_N2S_P<2>	D20	DMI2RXP	
84 9 IN DMI_N2S_P<3>	H18	DMI3RXP	
84 9 OUT DMI_S2N_N<0>	J22	DMI0TXN	
84 9 OUT DMI_S2N_N<1>	G22	DMI1TXN	
84 9 OUT DMI_S2N_N<2>	H24	DMI2TXN	
84 9 OUT DMI_S2N_N<3>	L24	DMI3TXN	
84 9 OUT DMI_S2N_P<0>	H22	DMI0TXP	
84 9 OUT DMI_S2N_P<1>	F22	DMI1TXP	
84 9 OUT DMI_S2N_P<2>	G24	DMI2TXP	
84 9 OUT DMI_S2N_P<3>	K24	DMI3TXP	
85 PCH_DMI_COMP	C21	DMI_ZCOMP	
SHORT THESE TWO PINS VERY NEAR THE PINS PLACE THE RESISTOR VERY CLOSE TO COMMON POINT	D21	DMI_IRCOMP	

FDI

FDI_RXN0	K30	TP_PCH_FDI_RX_N<0> 7
FDI_RXN1	H30	TP_PCH_FDI_RX_N<1> 7
FDI_RXN2	D31	TP_PCH_FDI_RX_N<2> 7
FDI_RXN3	F31	TP_PCH_FDI_RX_N<3> 7
FDI_RXN4	K31	TP_PCH_FDI_RX_N<4> 7
FDI_RXN5	C30	TP_PCH_FDI_RX_N<5> 7
FDI_RXN6	A33	TP_PCH_FDI_RX_N<6> 7
FDI_RXN7	C33	TP_PCH_FDI_RX_N<7> 7
FDI_RXP0	J30	TP_PCH_FDI_RX_P<0> 7
FDI_RXP1	G30	TP_PCH_FDI_RX_P<1> 7
FDI_RXP2	D32	TP_PCH_FDI_RX_P<2> 7
FDI_RXP3	G31	TP_PCH_FDI_RX_P<3> 7
FDI_RXP4	J31	TP_PCH_FDI_RX_P<4> 7
FDI_RXP5	B31	TP_PCH_FDI_RX_P<5> 7
FDI_RXP6	B32	TP_PCH_FDI_RX_P<6> 7
FDI_RXP7	B34	TP_PCH_FDI_RX_P<7> 7
FDI_INT	B36	TP_PCH_FDI_INT 7
FDI_FSYNC0	E34	TP_PCH_FDI_FSYNC<0> 7
FDI_FSYNC1	E36	TP_PCH_FDI_FSYNC<1> 7
FDI_LSYNC0	C35	TP_PCH_FDI_LSYNC<0> 7
FDI_LSYNC1	D35	TP_PCH_FDI_LSYNC<1> 7

SYSTEM POWER MANAGEMENT

91 46 27 IN PM_SYSRST_L	AL38	SYS_RESET*	
91 64 IN PM_SYS_PWRGD	AT38	SYS_PWROK	
91 64 IN PM_PCH_PWRGD	AM24	PWROK	
91 64 IN PM_ME_PWRGD	AL33	MEPWROK	
91 14 IN PM_LAN_PWRGD	AY31	LAN_RST*	
91 10 OUT PM_MEM_PWRGD	AW32	DRAMPWROK	
91 63 IN PM_RSMRST_PCH_L	AL24	RSMRST*	
91 PM_SUS_PWR_ACK	AT37	SUS_PWR_DN_ACK/GPIO30	
91 46 24 IN PM_PWRBTN_L	AK36	PWRBTN* (IPU)	
18 IN PCH_ACPRESENT_GPIO31	AP40	ACPRESENT/GPIO31	
91 46 14 IN PM_BATLOW_L	AY34	GPIO72	
PCH_RI_L	AT33	RI*	

WAKE*	AR33	PCIE_WAKE_L	IN 18 33 36
GPIO32	AJ40	PM_CLKRUN_L	BI 14 46 48 91
SUS_STAT*/GPIO61	AK31	LPC_PWRDWN_L	OUT 46 48
SUSCLK/GPIO62	AH31	PM_CLK32K_SUSCLK_R	OUT 8 85 91
SLP_S5*/GPIO63	AU36	PM_SLP_S5_L	OUT 47 91
SLP_S4*	AP35	PM_SLP_S4_L	OUT 18 47 91
SLP_S3*	AV35	PM_SLP_S3_L	OUT 5 26 36 46 47 63 64 81 91
SLP_M*	AT36	PM_SLP_M_L	OUT 63 91
TP23	AH35	TP_PM_SLP_DSW_L	
PMSYNCH	C37	PM_SYNC	OUT 10 91
SLP_LAN*/GPIO29	BA35	TP_SLP_LAN_L (KEEPING TP, IF NEED TO USE IT LATER)	

R1909 10K 1% 1/16W MF-LF 402

=PP3V3_S5_PCH 5 17 18 23

R1961 10K 1% 1/16W MF-LF 402

NOSTUFF
R1960 0 5% 1/16W MF-LF 402

47 46 SMC_ADAPTER_EN — PCH_ACPRESENT_GPIO31 18

R1966 33 5% 1/16W MF-LF 402

91 47 18 PM_SLP_S4_L (TO SMC) — PM_SLP_S4_1_L (To U6900) 63 91

=PP3V3_S5_PCH 5 17 18 23

R1925 1K 1% 1/16W MF-LF 402

PCIE_WAKE_L 18 33 36

IBEX-PEAK-DESKTOP

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DIGITAL DISPLAY INTERFACE

SDVO_TVCLKINN	L7	TP_SDVO_TVCLKINN 7
SDVO_TVCLKINP	L6	TP_SDVO_TVCLKINP 7
SDVO_STALLN	P3	TP_SDVO_STALLN 7
SDVO_STALLP	N2	TP_SDVO_STALLP 7
SDVO_INTN	N4	TP_SDVO_INTN 7
SDVO_INTP	M3	TP_SDVO_INTP 7
(IPD) SDVO_CTRLCLK	AB13	TP_DP_IG_B_DDC_CLK 7
(IPD) SDVO_CTRLDATA	AB12	TP_DP_IG_B_DDC_DATA 7
DDPB_AUXN	L2	TP_DP_IG_B_AUX_N 7
DDPB_AUXP	M1	TP_DP_IG_B_AUX_P 7
DDPB_HPD	J1	TP_DP_IG_B_HPD 7
DDPB_0N	J8	TP_DP_IG_B_MLN<0> 7
DDPB_0P	K10	TP_DP_IG_B_MLP<0> 7
DDPB_1N	J11	TP_DP_IG_B_MLN<1> 7
DDPB_1P	K11	TP_DP_IG_B_MLP<1> 7
DDPB_2N	F6	TP_DP_IG_B_MLN<2> 7
DDPB_2P	H6	TP_DP_IG_B_MLP<2> 7
DDPB_3N	H4	TP_DP_IG_B_MLN<3> 7
DDPB_3P	G4	TP_DP_IG_B_MLP<3> 7
(IPU) DDPC_CTRLCLK	AB10	TP_DP_IG_C_CTRL_CLK 7
(IPD) DDPC_CTRLDATA	AB11	TP_DP_IG_C_CTRL_DATA 7
DDPC_AUXN	L10	TP_DP_IG_C_AUX_N 7
DDPC_AUXP	L9	TP_DP_IG_C_AUX_P 7
DDPC_HPD	J3	TP_DP_IG_C_HPD 7
DDPC_0N	F4	TP_DP_IG_C_MLN<0> 7
DDPC_0P	E3	TP_DP_IG_C_MLP<0> 7
DDPC_1N	G3	TP_DP_IG_C_MLN<1> 7
DDPC_1P	F2	TP_DP_IG_C_MLP<1> 7
DDPC_2N	C4	TP_DP_IG_C_MLN<2> 7
DDPC_2P	B4	TP_DP_IG_C_MLP<2> 7
DDPC_3N	D2	TP_DP_IG_C_MLN<3> 7
DDPC_3P	D3	TP_DP_IG_C_MLP<3> 7
(IPU) DDPD_CTRLCLK	AB7	TP_DP_IG_D_CTRL_CLK 7
(IPD) DDPD_CTRLDATA	AB9	TP_DP_IG_D_CTRL_DATA 7
DDPD_AUXN	L4	TP_DP_IG_D_AUXN 7
DDPD_AUXP	K4	TP_DP_IG_D_AUXP 7
DDPD_HPD	H2	TP_DP_IG_D_HPD 7
DDPD_0N	B6	TP_DP_IG_D_MLN<0> 7
DDPD_0P	C5	TP_DP_IG_D_MLP<0> 7
DDPD_1N	D7	TP_DP_IG_D_MLN<1> 7
DDPD_1P	D6	TP_DP_IG_D_MLP<1> 7
DDPD_2N	G8	TP_DP_IG_D_MLN<2> 7
DDPD_2P	F8	TP_DP_IG_D_MLP<2> 7
DDPD_3N	G9	TP_DP_IG_D_MLN<3> 7
DDPD_3P	F9	TP_DP_IG_D_MLP<3> 7

EXTERNAL DP

INTERNAL DP

CRT

7 TP_CRT_IG_BLUE	AB2	CRT_BLUE	
7 TP_CRT_IG_GREEN	AC3	CRT_GREEN	
7 TP_CRT_IG_RED	AC1	CRT_RED	
7 TP_CRT_IG_DDC_CLK	AG2	CRT_DDC_CLK	
7 TP_CRT_IG_DDC_DATA	AG4	CRT_DDC_DATA	
7 TP_CRT_IG_HSYNC	AD4	CRT_HSYNC	
7 TP_CRT_IG_VSYNC	AD3	CRT_VSYNC	
PCH_DAC_IREF	AE2	DAC_IREF	
	AB4	CRT_IRTN	

R1951 1K 5% 1/16W MF-LF 402
PLACE CLOSE TO U1800 PIN

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCH DMI/FDI/GRAPHICS

Apple Inc.

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PCI

TP_PCI_AD<0>	AT9	AD0	
TP_PCI_AD<1>	AP11	AD1	
TP_PCI_AD<2>	AU6	AD2	
TP_PCI_AD<3>	AY10	AD3	
TP_PCI_AD<4>	AP9	AD4	
TP_PCI_AD<5>	AV8	AD5	
TP_PCI_AD<6>	AR9	AD6	
TP_PCI_AD<7>	AV7	AD7	
TP_PCI_AD<8>	AW9	AD8	
TP_PCI_AD<9>	AR3	AD9	
TP_PCI_AD<10>	AW7	AD10	
TP_PCI_AD<11>	AR8	AD11	
TP_PCI_AD<12>	AU3	AD12	
TP_PCI_AD<13>	AP2	AD13	
TP_PCI_AD<14>	AU1	AD14	
TP_PCI_AD<15>	AN3	AD15	
TP_PCI_AD<16>	AM2	AD16	
TP_PCI_AD<17>	AM11	AD17	
TP_PCI_AD<18>	AM4	AD18	
TP_PCI_AD<19>	AY8	AD19	
TP_PCI_AD<20>	AL10	AD20	
TP_PCI_AD<21>	AT5	AD21	
TP_PCI_AD<22>	AL2	AD22	
TP_PCI_AD<23>	AT2	AD23	
TP_PCI_AD<24>	AL4	AD24	
TP_PCI_AD<25>	AV10	AD25	
TP_PCI_AD<26>	AL9	AD26	
TP_PCI_AD<27>	AN7	AD27	
TP_PCI_AD<28>	AK7	AD28	
TP_PCI_AD<29>	AN6	AD29	
TP_PCI_AD<30>	AH12	AD30	
TP_PCI_AD<31>	AN11	AD31	
TP_PCI_C_BE_L<0>	AV3	C/BE0*	
TP_PCI_C_BE_L<1>	AY6	C/BE1*	
TP_PCI_C_BE_L<2>	AP5	C/BE2*	
TP_PCI_C_BE_L<3>	AW10	C/BE3*	
PCI_INTA_L	AT8	PIRQA*	
PCI_INTB_L	AR4	PIRQB*	
PCI_INTC_L	AT11	PIRQC*	
PCI_INTD_L	BA5	PIRQD*	
PCI_REQ0_L	AP4	REQ0*	
PCI_REQ1_L	AW5	REQ1*/GPIO50	
PCI_REQ2_L	AY4	REQ2*/GPIO52	
PCI_REQ3_L	AH8	REQ3*/GPIO54	
PCH_PCI_GNT0_L	AK11	GNT0* (IPU)	
PCH_PCI_GNT1_L	AK6	GNT1*/GPIO51	
PCH_PCI_GNT2_L	BA9	GNT2*/GPIO53	
PCH_PCI_GNT3_L	AM3	GNT3*/GPIO55	
PCI_INTE_L	AU8	PIRQE*/GPIO2	
AUD_IP_PERIPHERAL_DET	AH7	PIRQF*/GPIO3	
PCI_INTG_L	AP12	PIRQG*/GPIO4	
AUD_I2C_INT_L	AW4	PIRQH*/GPIO5	
TP_PCI_RESET_L	AH10	PCIRST*	
PCI_SERR_L	AV6	SERR*	
PCI_PERR_L	AT4	PERR*	
PCI_IRDY_L	AP7	IRDY*	
TP_PCI_PAR	AP6	PAR	
PCI_DEVSEL_L	AT6	DEVSEL*	
PCI_FRAME_L	AL7	FRAME*	
PCI_PLOCK_L	AK12	PLOCK*	
PCI_STOP_L	AN8	STOP*	
PCI_TRDY_L	AL6	TRDY*	
TP_PCI_PME_L	AH11	PME* (IPU)	
PLT_RESET_L	AV34	PLTRST*	
LPC_CLK33M_SMC_R	AF6	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R	AD7	CLKOUT_PCI1	
TP_PCI_CLK33M_OUT2	AF9	CLKOUT_PCI2	
TP_PCI_CLK33M_OUT3	AD9	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT	AD12	CLKOUT_PCI4	

=PP3V3_S0_PCH_GPIO

R2010 10K 5% 1/16W MF-LF 402 — PCI_INTA_L
R2011 10K 5% 1/16W MF-LF 402 — PCI_INTB_L
R2012 10K 5% 1/16W MF-LF 402 — PCI_INTC_L
R2013 10K 5% 1/16W MF-LF 402 — PCI_INTD_L
R2015 10K 5% 1/16W MF-LF 402 — PCI_REQ0_L
R2016 10K 5% 1/16W MF-LF 402 — PCI_REQ1_L
R2017 10K 5% 1/16W MF-LF 402 — PCI_REQ2_L
R2018 10K 5% 1/16W MF-LF 402 — PCI_REQ3_L
R2030 10K 5% 1/16W MF-LF 402 — PCI_INTE_L
R2031 10K 5% 1/16W MF-LF 402 — PCI_INTG_L
R2020 10K 5% 1/16W MF-LF 402 — PCI_SERR_L
R2021 10K 5% 1/16W MF-LF 402 — PCI_PERR_L
R2022 10K 5% 1/16W MF-LF 402 — PCI_IRDY_L
R2023 10K 5% 1/16W MF-LF 402 — PCI_DEVSEL_L
R2024 10K 5% 1/16W MF-LF 402 — PCI_FRAME_L
R2027 10K 5% 1/16W MF-LF 402 — PCI_PLOCK_L
R2025 10K 5% 1/16W MF-LF 402 — PCI_STOP_L
R2026 10K 5% 1/16W MF-LF 402 — PCI_TRDY_L

NVRAM

NV_CE0*	H36	TP_NV_CE_L<0>
NV_CE1*	H35	TP_NV_CE_L<1>
NV_CE2*	P32	TP_NV_CE_L<2>
NV_CE3*	E41	TP_NV_CE_L<3>
NV_DQS0	P36	TP_NV_DQS<0>
NV_DQS1	F40	TP_NV_DQS<1>
NV_DQ0/NV_IO0	T33	TP_NV_DQ<0>
NV_DQ1/NV_IO1	P35	TP_NV_DQ<1>
NV_DQ2/NV_IO2	T31	TP_NV_DQ<2>
NV_DQ3/NV_IO3	P33	TP_NV_DQ<3>
NV_DQ4/NV_IO4	M35	TP_NV_DQ<4>
NV_DQ5/NV_IO5	L33	TP_NV_DQ<5>
NV_DQ6/NV_IO6	M36	TP_NV_DQ<6>
NV_DQ7/NV_IO7	M34	TP_NV_DQ<7>
NV_DQ8/NV_IO8	M30	TP_NV_DQ<8>
NV_DQ9/NV_IO9	F36	TP_NV_DQ<9>
NV_DQ10/NV_IO10	H33	TP_NV_DQ<10>
NV_DQ11/NV_IO11	F37	TP_NV_DQ<11>
NV_DQ12/NV_IO12	E39	TP_NV_DQ<12>
NV_DQ13/NV_IO13	G33	TP_NV_DQ<13>
NV_DQ14/NV_IO14	D40	TP_NV_DQ<14>
NV_DQ15/NV_IO15	F33	TP_NV_DQ<15>
(IPD) NV_ALE	J34	TP_NV_ALE
(IPD) NV_CLE	L35	TP_NV_CLE
NV_RCOMP	L36	TP_NV_RCOMP
(IPU) NV_RB*	M32	TP_NV_RB_L
NV_WR0_RE*	J36	TP_NV_WR_RE_L<0>
NV_WR1_RE*	J35	TP_NV_WR_RE_L<1>
NV_WE_CK0*	M31	TP_NV_WE_CK_L<0>
NV_WE_CK1*	F38	TP_NV_WE_CK_L<1>

USB

NOTE: Internal pull-downs on all USB pins

EHCI1 (OPD)

USBP0N	AW25	USB_HUB1_UP_N	USB HUB 1
USBP0P	AY25	USB_HUB1_UP_P	
USBP1N	BA23	TP_USB_1N	Unused
USBP1P	AY24	TP_USB_1P	
USBP2N	AW23	TP_USB_2N	Unused
USBP2P	AY22	TP_USB_2P	
USBP3N	AR22	TP_USB_3N	Unused
USBP3P	AP22	TP_USB_3P	
USBP4N	AV21	TP_USB_4N	Unused
USBP4P	AV22	TP_USB_4P	
USBP5N	AY20	TP_USB_5N	Unused
USBP5P	AW21	TP_USB_5P	
USBP6N	AK20	TP_USB_6N	Unused
USBP6P	AL20	TP_USB_6P	
USBP7N	AV20	TP_USB_7N	Unused
USBP7P	AW19	TP_USB_7P	

EHCI2 (OPD)

USBP8N	BA19	USB_HUB2_UP_N	USB HUB 2
USBP8P	AY18	USB_HUB2_UP_P	
USBP9N	AM20	TP_USB_9N	Unused
USBP9P	AN20	TP_USB_9P	
USBP10N	AV17	TP_USB_10N	Unused
USBP10P	AV18	TP_USB_10P	
USBP11N	AR20	TP_USB_11N	Unused
USBP11P	AT20	TP_USB_11P	
USBP12N	AK18	TP_USB_12N	Unused
USBP12P	AL18	TP_USB_12P	
USBP13N	AY17	TP_USB_13N	Unused
USBP13P	BA16	TP_USB_13P	

USBRBIAS* AY15 — PCH_USB_RBIAS
USBRBIAS AV15
TIE TRACES TOGETHER CLOSE TO PINS

R2070 22.6 1% 1/16W MF-LF 402
PLACE THE RESISTOR CLOSE TO COMMON POINT

OC0*/GPIO59	AT31	PCH_GPIO59_OC0_L
OC1*/GPIO40	AT30	USB_HUB_SOFT_RESET_L
OC2*/GPIO41	AK28	PCH_GPIO41_OC2_L
OC3*/GPIO42	AP30	PCH_GPIO42_OC3_L
OC4*/GPIO43	AP31	PCH_GPIO43_OC4_L
OC5*/GPIO9	AL28	PCH_GPIO9_OC5_L
OC6*/GPIO10	AL30	PCH_GPIO10_OC6_L
OC7*/GPIO14	AM30	PCH_GPIO14_OC7_L

=PP3V3_S5_PCH_GPIO

NO STUFF R2061 10K 5% 1/16W MF-LF 402
R2060 10K 5% 1/16W MF-LF 402
R2062 10K 5% 1/16W MF-LF 402
R2067 10K 5% 1/16W MF-LF 402
R2065 10K 5% 1/16W MF-LF 402
R2064 10K 5% 1/16W MF-LF 402
R2066 10K 5% 1/16W MF-LF 402
R2068 10K 5% 1/16W MF-LF 402

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

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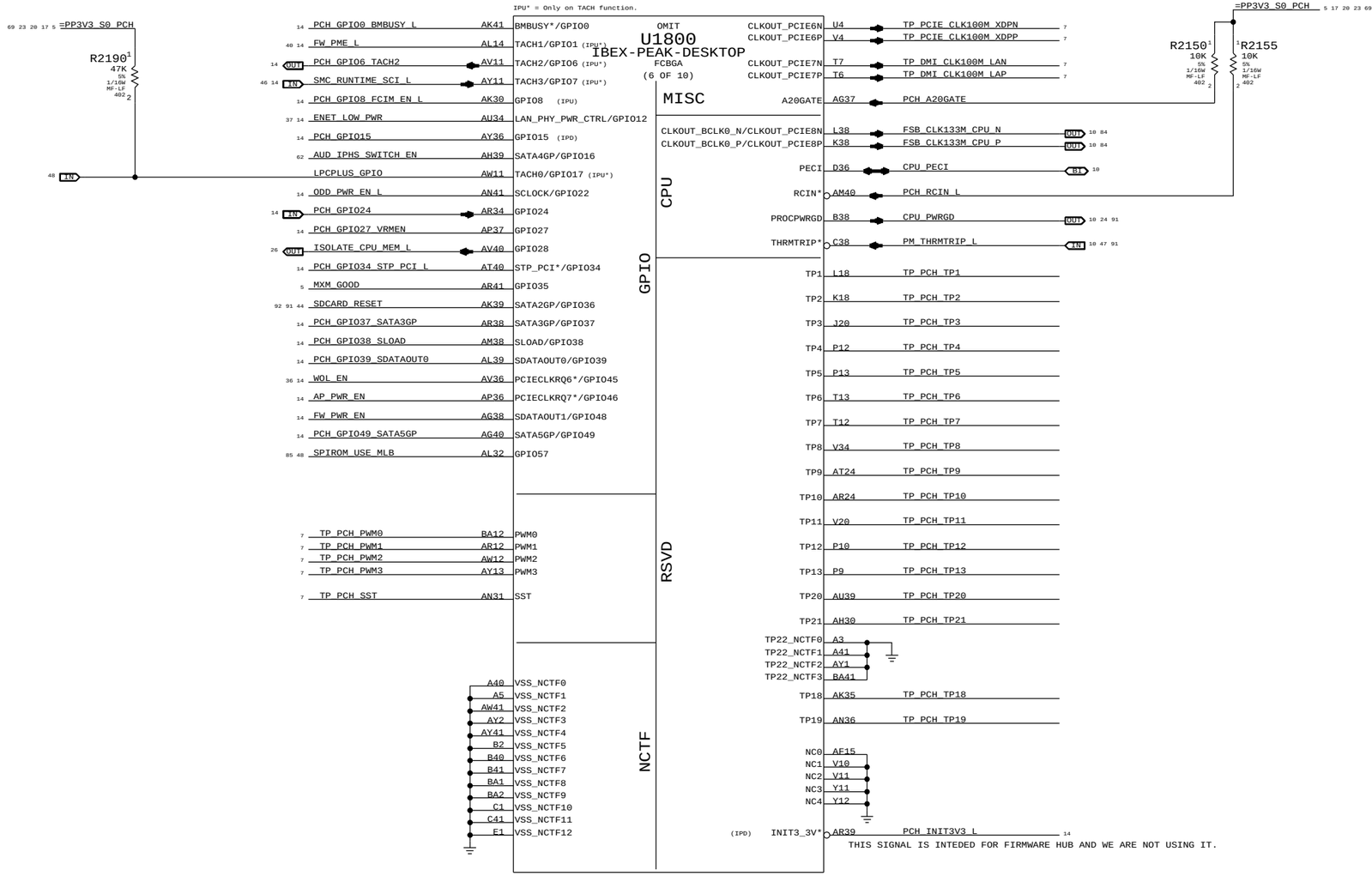

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: PCH MISC

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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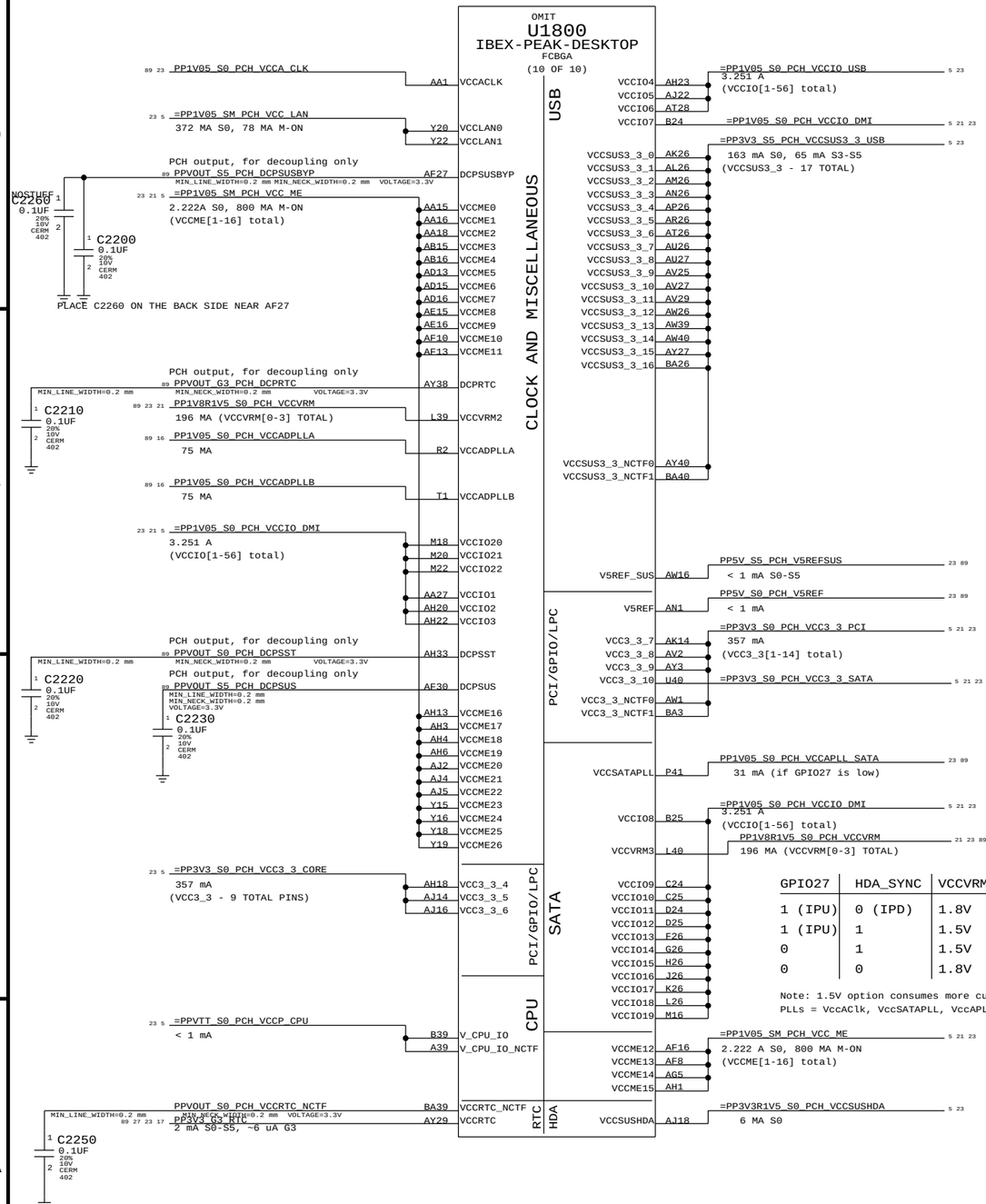

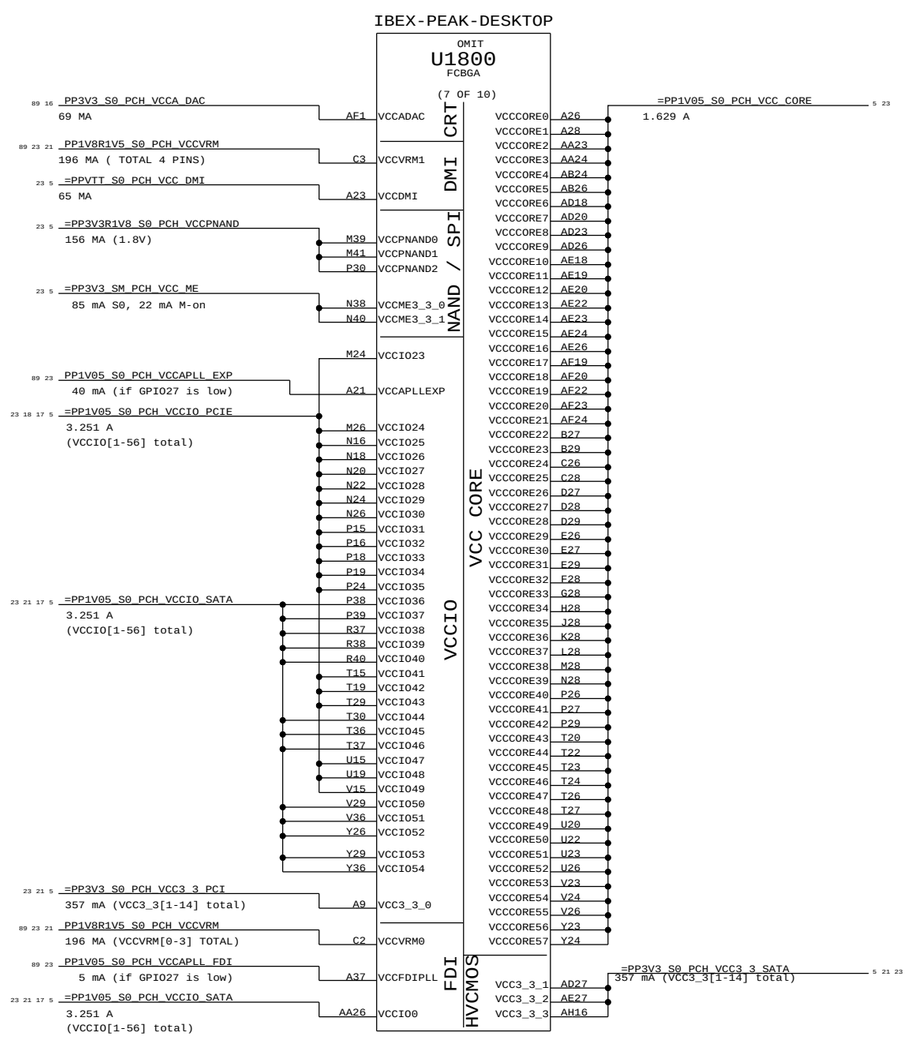

PAGE TITLE	PCH POWER
	Apple Inc.
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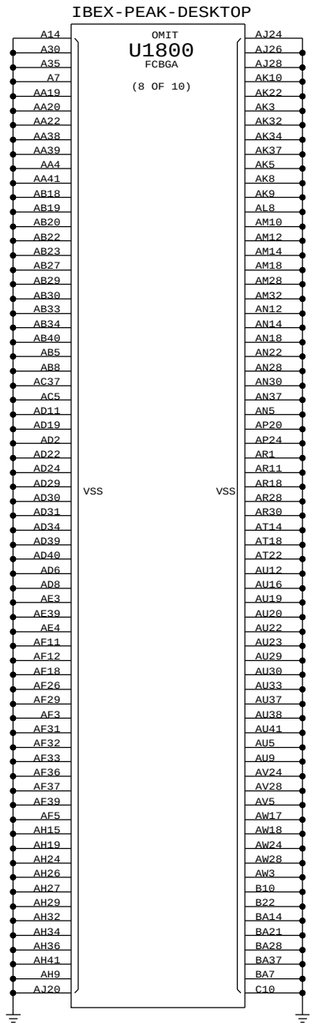

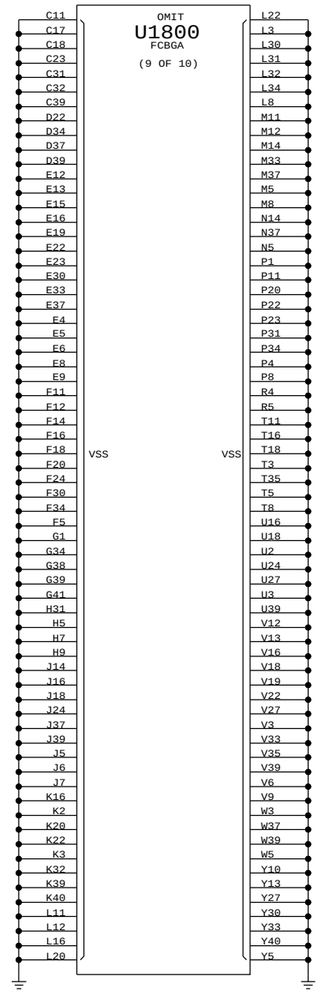

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE

PCH GROUNDS

Apple Inc.

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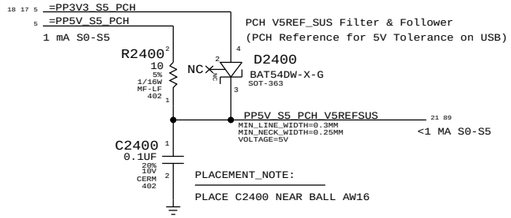

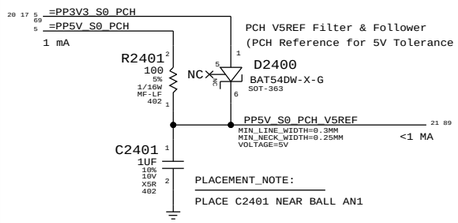

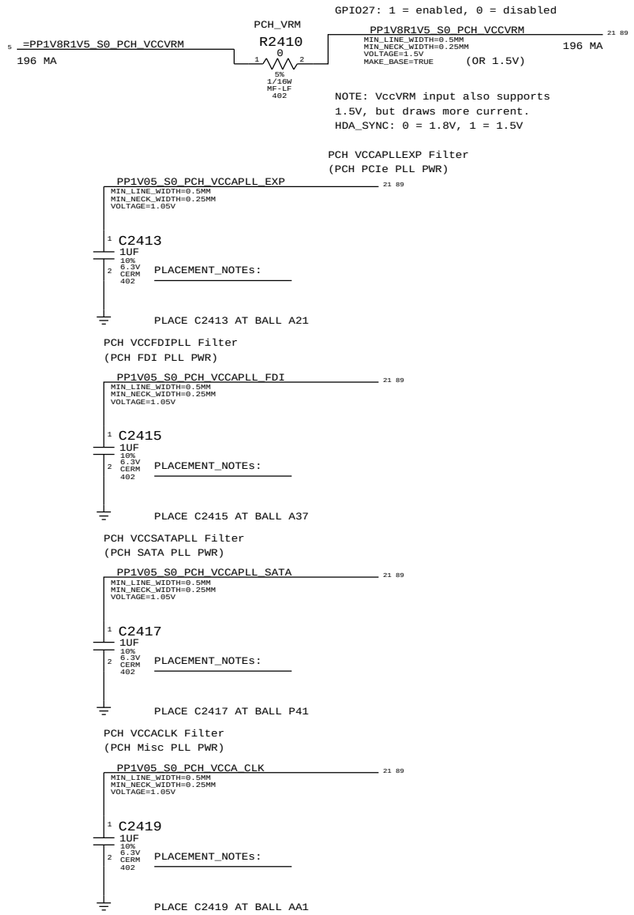

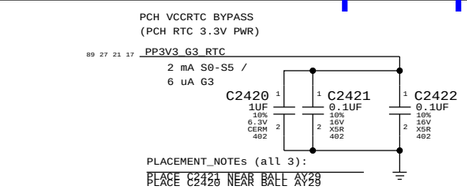

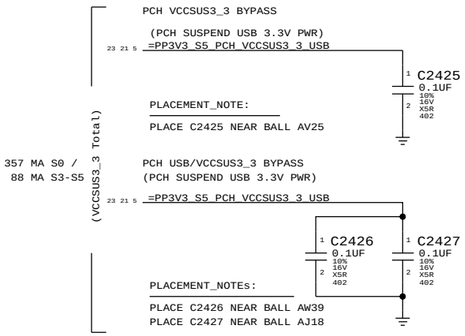

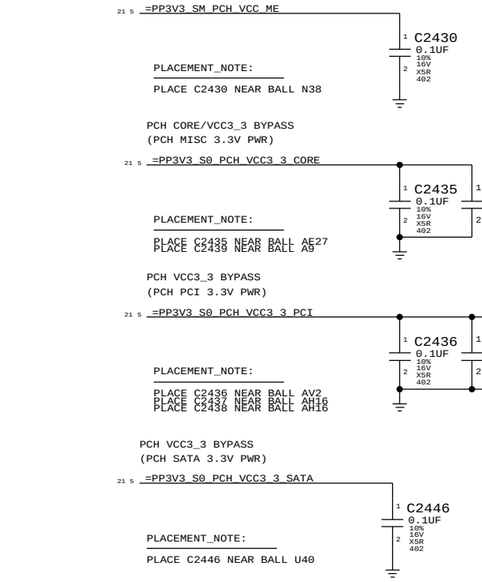

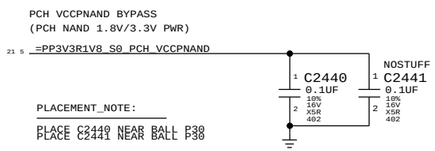

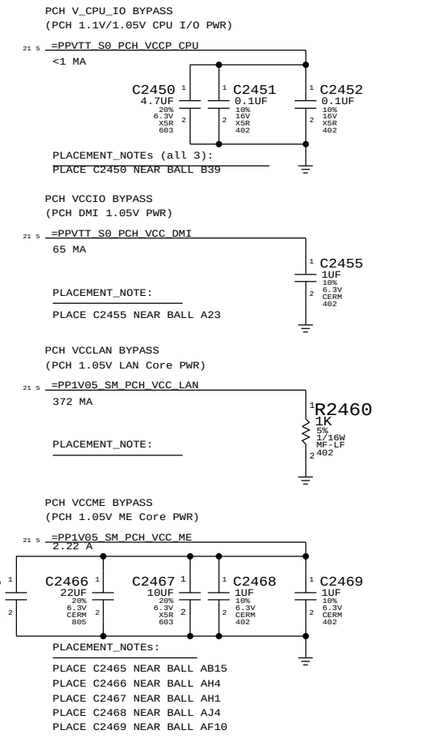

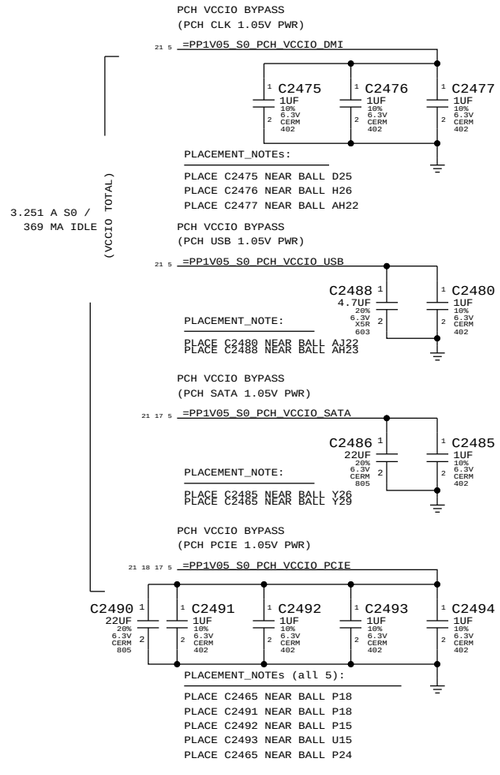

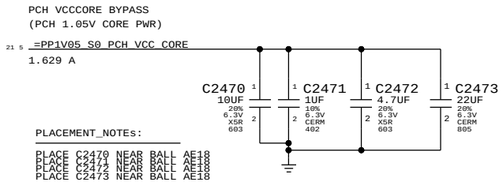

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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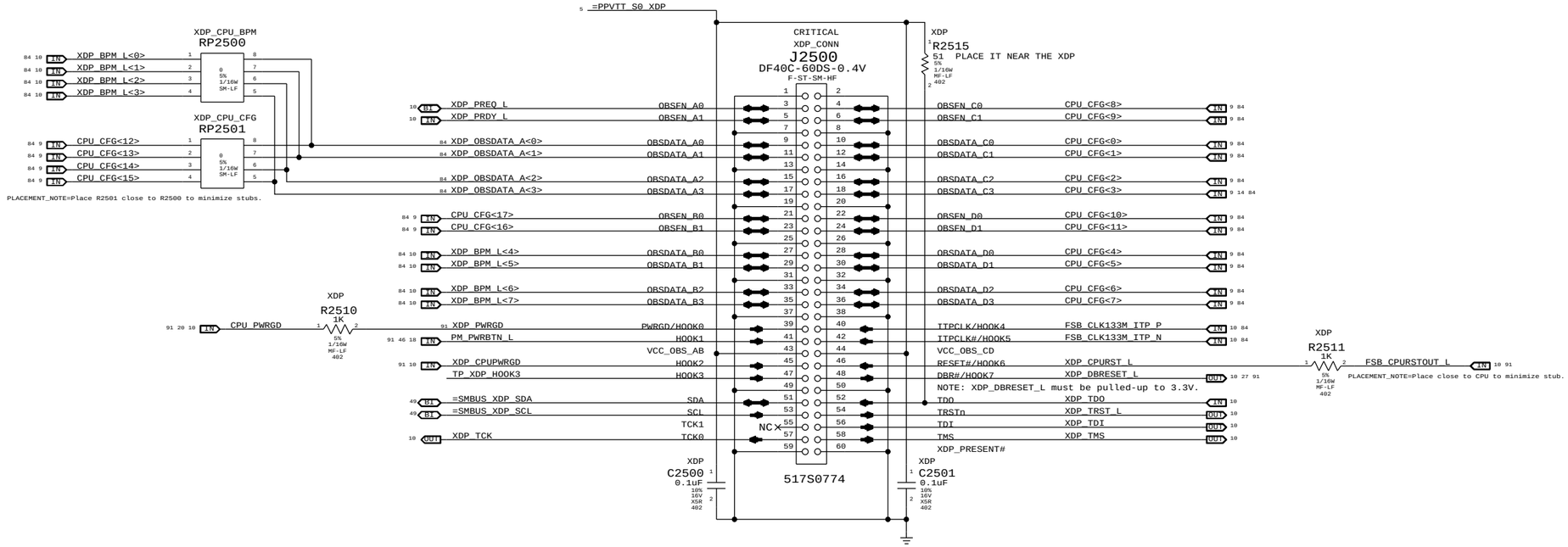
PROCESSOR MINI XDP



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PAGE TITLE
EXTENDED DEBUG PORT(XDP)

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
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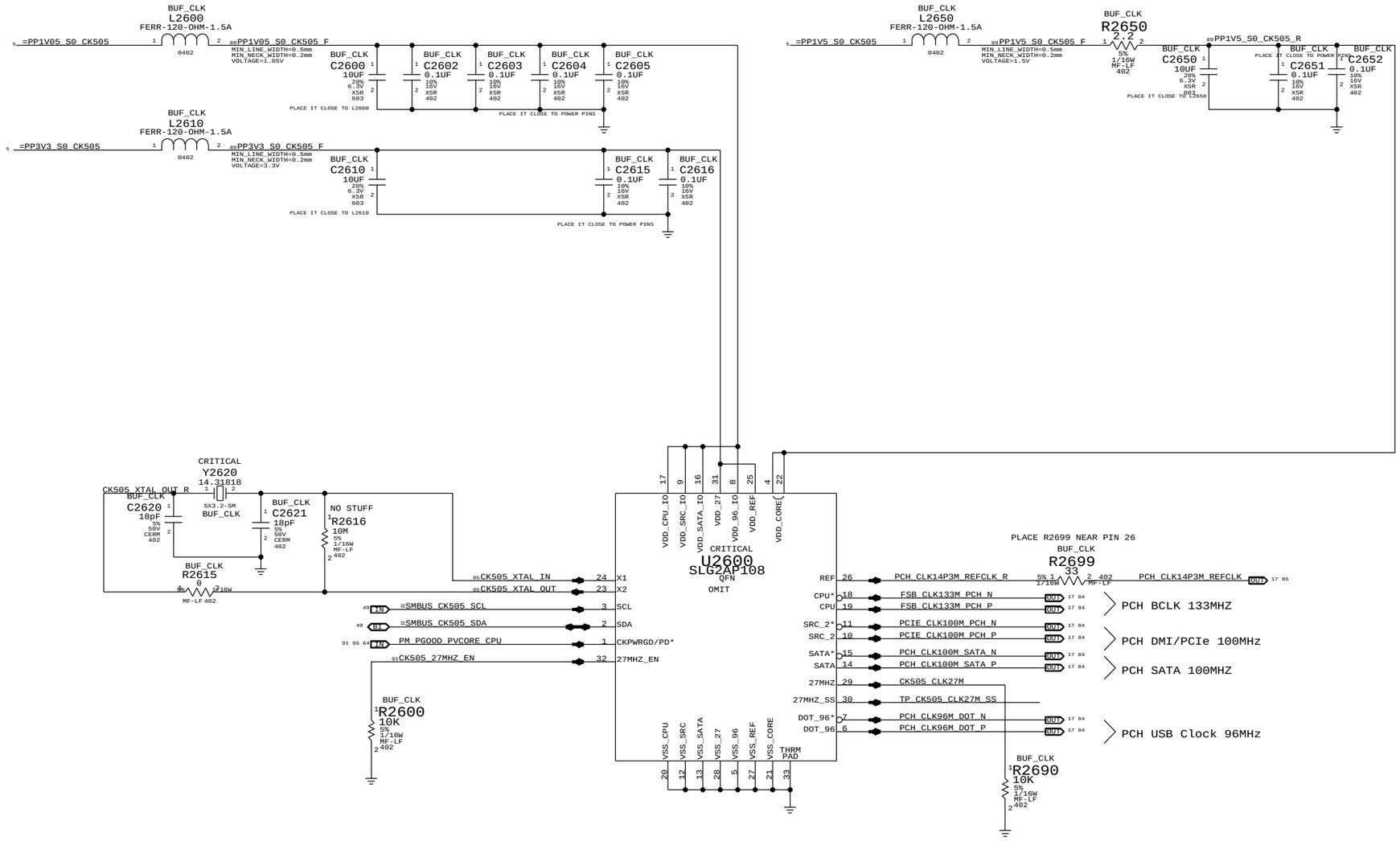

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PAGE TITLE
CLOCK (CK505)

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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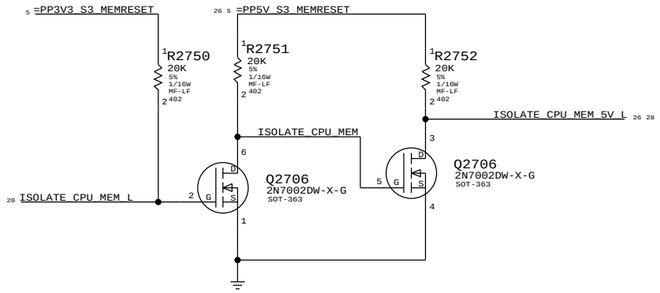
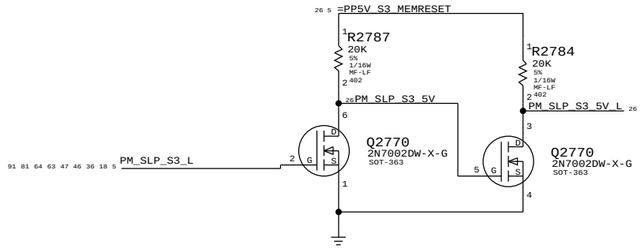
DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

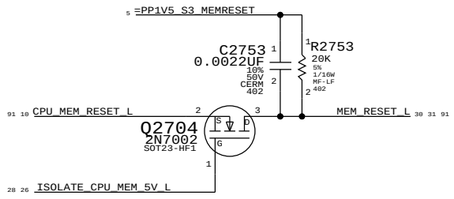
	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

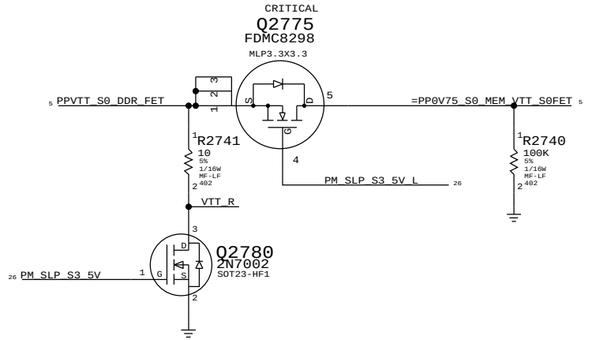
BUFFER ISOLATE_CPU_MEM_L TO 5V





MEM RESET ISOLATION





SYNC_MASTER=MATT	SYNC_DATE=01/06/2010
PAGE TITLE	DDR3 RESET
Apple Inc.	DRAWING NUMBER 051-8337 SIZE D
	REVISION A.0.0
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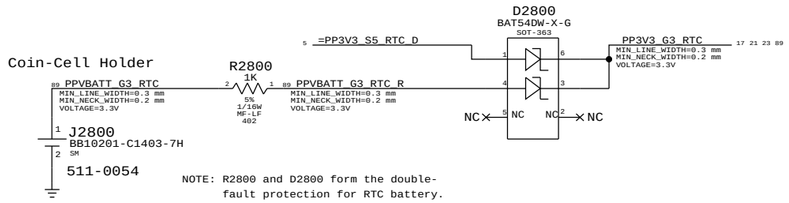
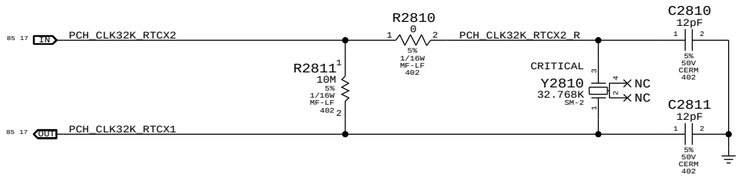
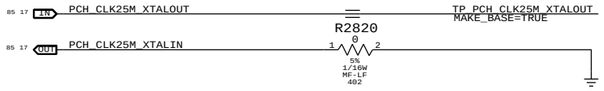
RTC Power Sources



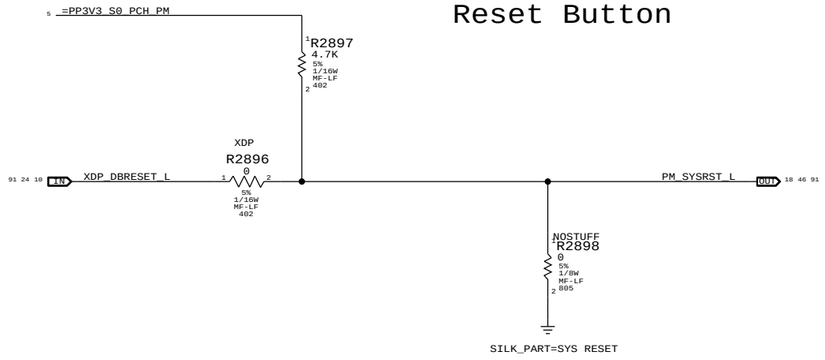
PCH RTC Crystal



UNUSED PCH 25MHZ CRYSTAL

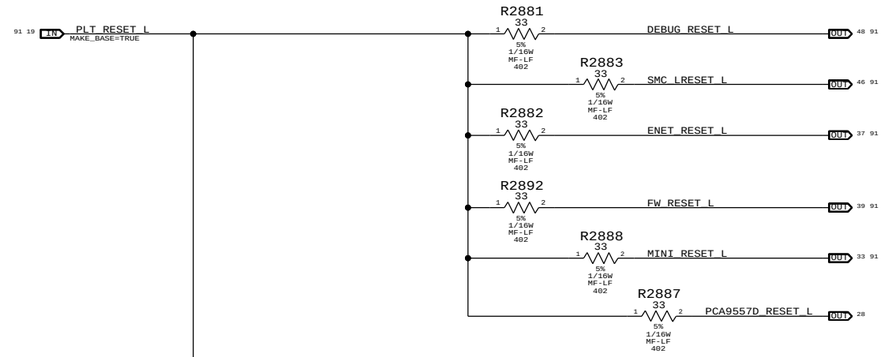


Reset Button



Platform Reset Connections

Unbuffered



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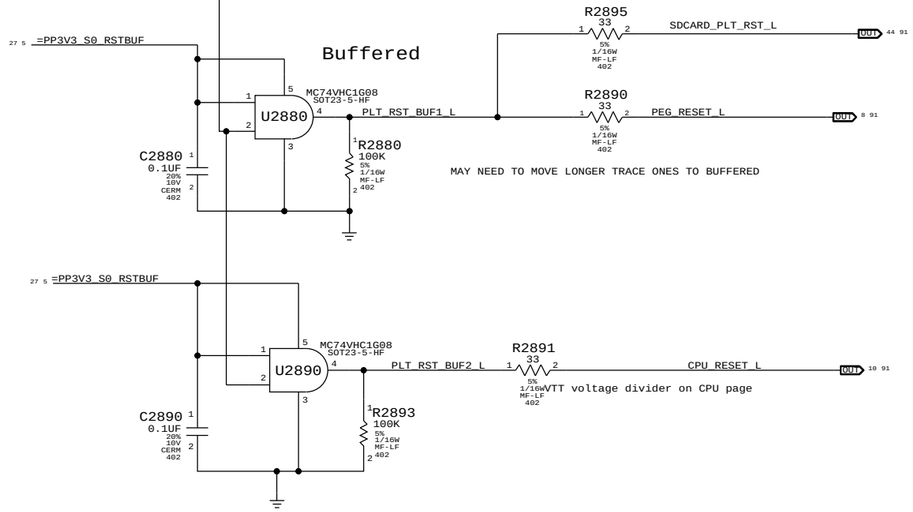

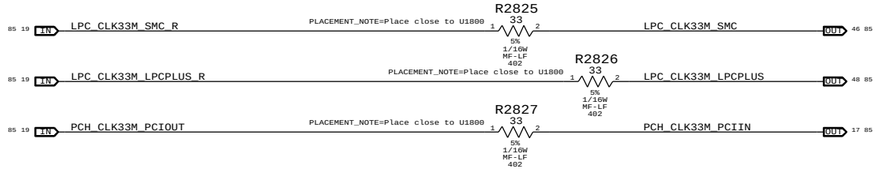

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Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
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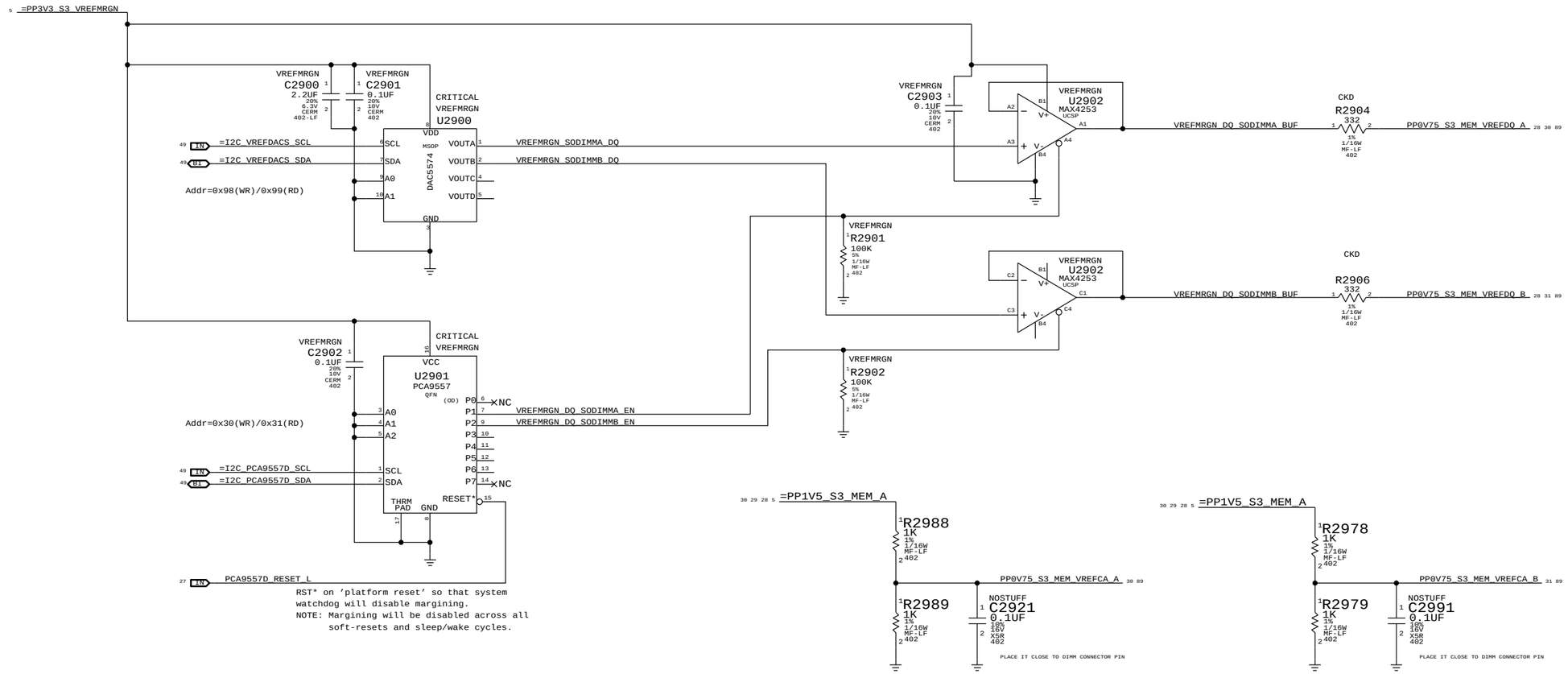
Page Notes

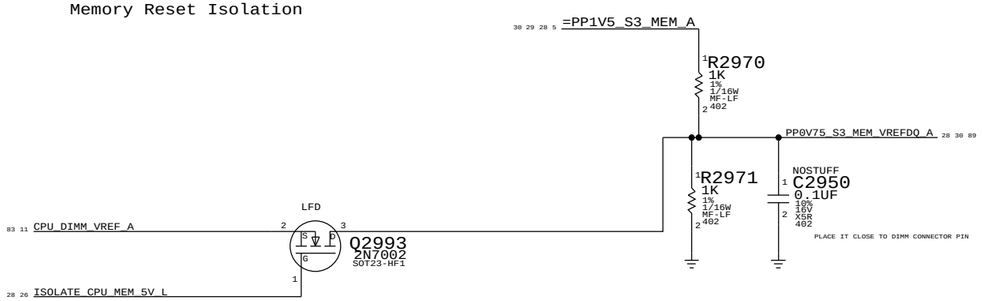
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN

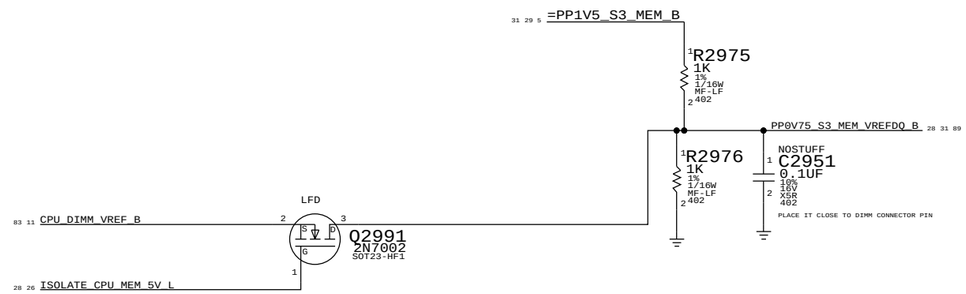
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.



Memory Reset Isolation





	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=MATT SYNC_DATE=01/06/2010

PAGE TITLE: DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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DIMM A (FURTHER FROM CPU)

CAPS TO COUPLE CPU 1V5_MEM

DIMM B (CLOSER TO CPU)

29 15 12 10 5 =PP1V5_CPU_MEM

C3016 1UF 10% 6.3V CERM 402
C3017 1UF 10% 6.3V CERM 402
C3018 1UF 10% 6.3V CERM 402
C3019 1UF 10% 6.3V CERM 402
C3010 1UF 10% 6.3V CERM 402
C3025 1UF 10% 6.3V CERM 402
C3026 1UF 10% 6.3V CERM 402
C3027 1UF 10% 6.3V CERM 402
C3028 1UF 10% 6.3V CERM 402
C3029 1UF 10% 6.3V CERM 402
C3020 1UF 10% 6.3V CERM 402
C3021 1UF 10% 6.3V CERM 402
C3022 1UF 10% 6.3V CERM 402
C3023 1UF 10% 6.3V CERM 402
C3014 1UF 10% 6.3V CERM 402
C3030 1UF 10% 6.3V CERM 402
C3031 1UF 10% 6.3V CERM 402
C3032 1UF 10% 6.3V CERM 402
C3033 1UF 10% 6.3V CERM 402

EXTRA DECOUPLING CAPS FOR CPU MEM RAIL

29 15 12 10 5 =PP1V5_CPU_MEM

C3041 1UF 10% 6.3V CERM 402
C3042 1UF 10% 6.3V CERM 402
C3044 1UF 10% 6.3V CERM 402
C3046 1UF 10% 6.3V CERM 402
C3040 1UF 10% 6.3V CERM 402
C3043 1UF 10% 6.3V CERM 402
C3045 1UF 10% 6.3V CERM 402
C3047 1UF 10% 6.3V CERM 402
C3048 1UF 10% 6.3V CERM 402
C3049 1UF 10% 6.3V CERM 402
C3090 1UF 10% 6.3V CERM 402
C3091 1UF 10% 6.3V CERM 402
C3092 1UF 10% 6.3V CERM 402
C3093 1UF 10% 6.3V CERM 402
C3094 1UF 10% 6.3V CERM 402

29 15 12 10 5 =PP1V5_CPU_MEM

C30A0 1UF 10% 6.3V CERM 402
C30A1 1UF 10% 6.3V CERM 402
C30A2 1UF 10% 6.3V CERM 402
C30A3 1UF 10% 6.3V CERM 402
C30A4 1UF 10% 6.3V CERM 402
C30A5 1UF 10% 6.3V CERM 402
C30A6 1UF 10% 6.3V CERM 402
C30A7 1UF 10% 6.3V CERM 402
C30A8 1UF 10% 6.3V CERM 402
C30A9 1UF 10% 6.3V CERM 402
C30AA 1UF 10% 6.3V CERM 402
C30AB 1UF 10% 6.3V CERM 402
C30AC 1UF 10% 6.3V CERM 402
C30AD 1UF 10% 6.3V CERM 402
C30AE 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

30 28 5 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V X5R 603
C3051 10UF 20% 6.3V X5R 603
C3052 1UF 10% 6.3V CERM 402
C3053 1UF 10% 6.3V CERM 402
C3054 1UF 10% 6.3V CERM 402
C3055 1UF 10% 6.3V CERM 402
C3056 1UF 10% 6.3V CERM 402
C3057 1UF 10% 6.3V CERM 402
C3058 1UF 10% 6.3V CERM 402
C3059 1UF 10% 6.3V CERM 402
C3060 1UF 10% 6.3V CERM 402
C3061 1UF 10% 6.3V CERM 402
C3062 1UF 10% 6.3V CERM 402
C3063 1UF 10% 6.3V CERM 402
C3064 1UF 10% 6.3V CERM 402
C3065 1UF 10% 6.3V CERM 402
C3066 1UF 10% 6.3V CERM 402
C3067 1UF 10% 6.3V CERM 402
C3068 1UF 10% 6.3V CERM 402
C3069 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

31 28 5 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V X5R 603
C3071 10UF 20% 6.3V X5R 603
C3072 1UF 10% 6.3V CERM 402
C3073 1UF 10% 6.3V CERM 402
C3074 1UF 10% 6.3V CERM 402
C3075 1UF 10% 6.3V CERM 402
C3076 1UF 10% 6.3V CERM 402
C3077 1UF 10% 6.3V CERM 402
C3078 1UF 10% 6.3V CERM 402
C3079 1UF 10% 6.3V CERM 402
C3080 1UF 10% 6.3V CERM 402
C3081 1UF 10% 6.3V CERM 402
C3082 1UF 10% 6.3V CERM 402
C3083 1UF 10% 6.3V CERM 402
C3084 1UF 10% 6.3V CERM 402
C3085 1UF 10% 6.3V CERM 402
C3086 1UF 10% 6.3V CERM 402
C3087 1UF 10% 6.3V CERM 402
C3088 1UF 10% 6.3V CERM 402
C3089 1UF 10% 6.3V CERM 402

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
MEMORY CAPS

Apple Inc.

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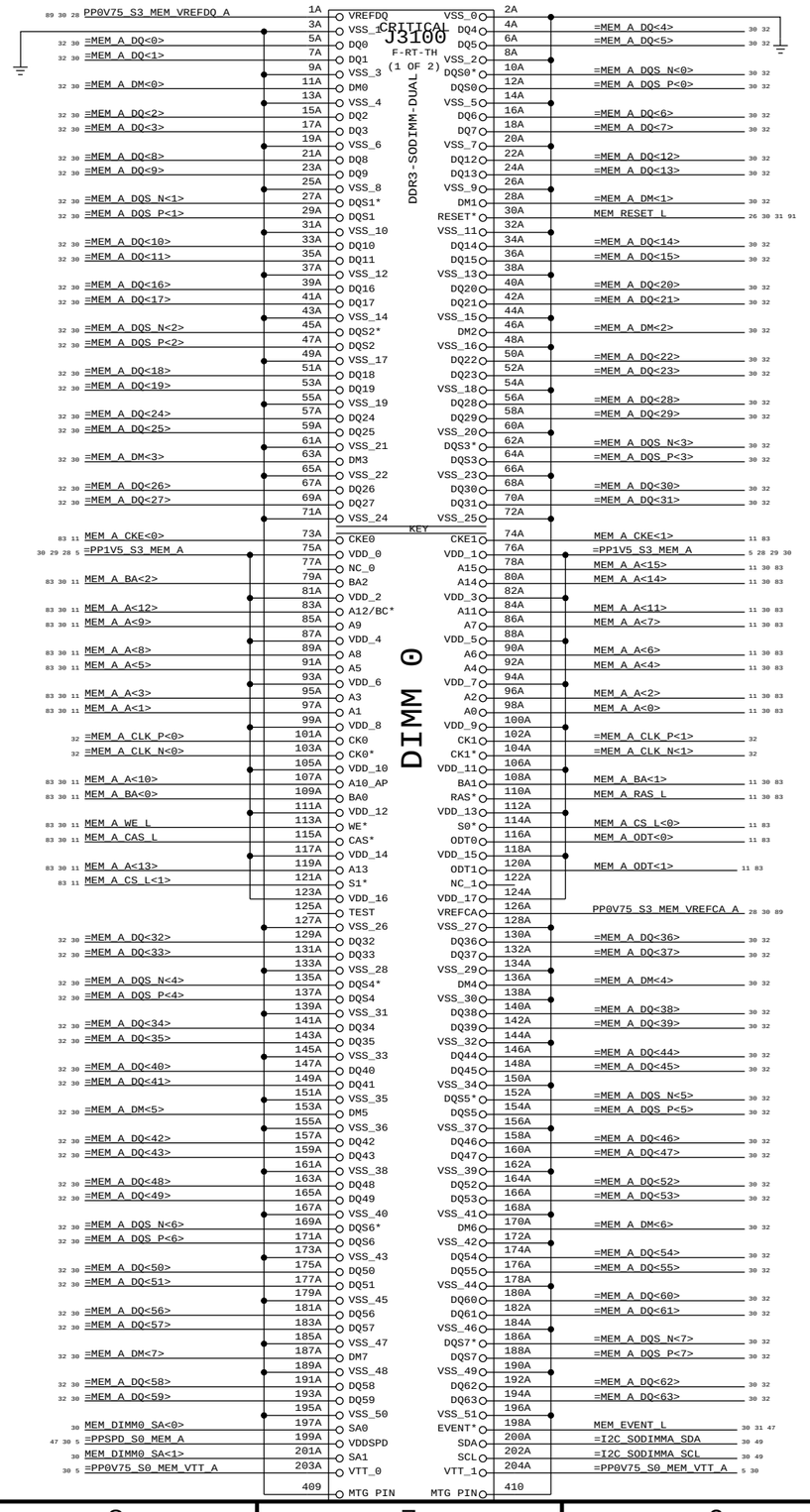

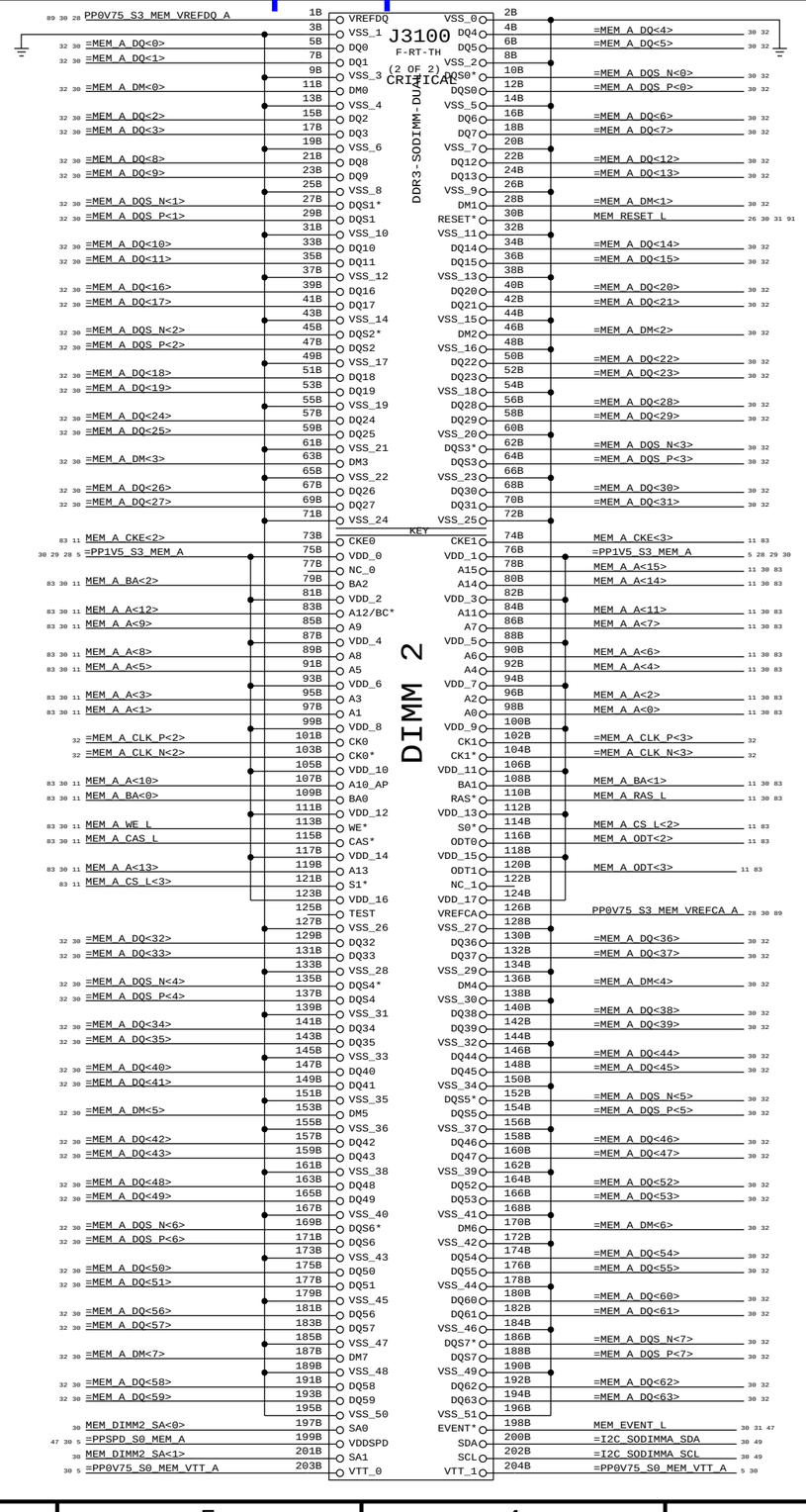

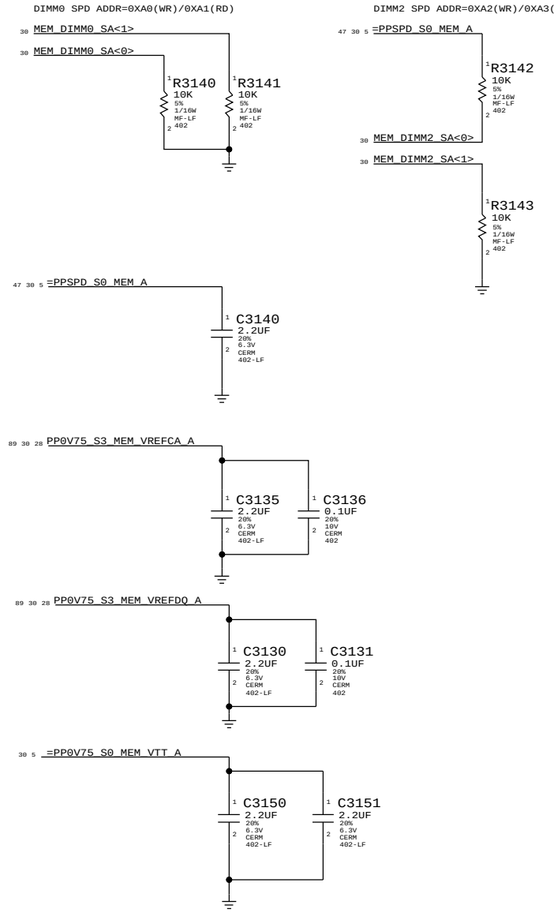

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
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PAGE TITLE
DDR3 SO-DIMMs 0 & 2

Apple Inc.

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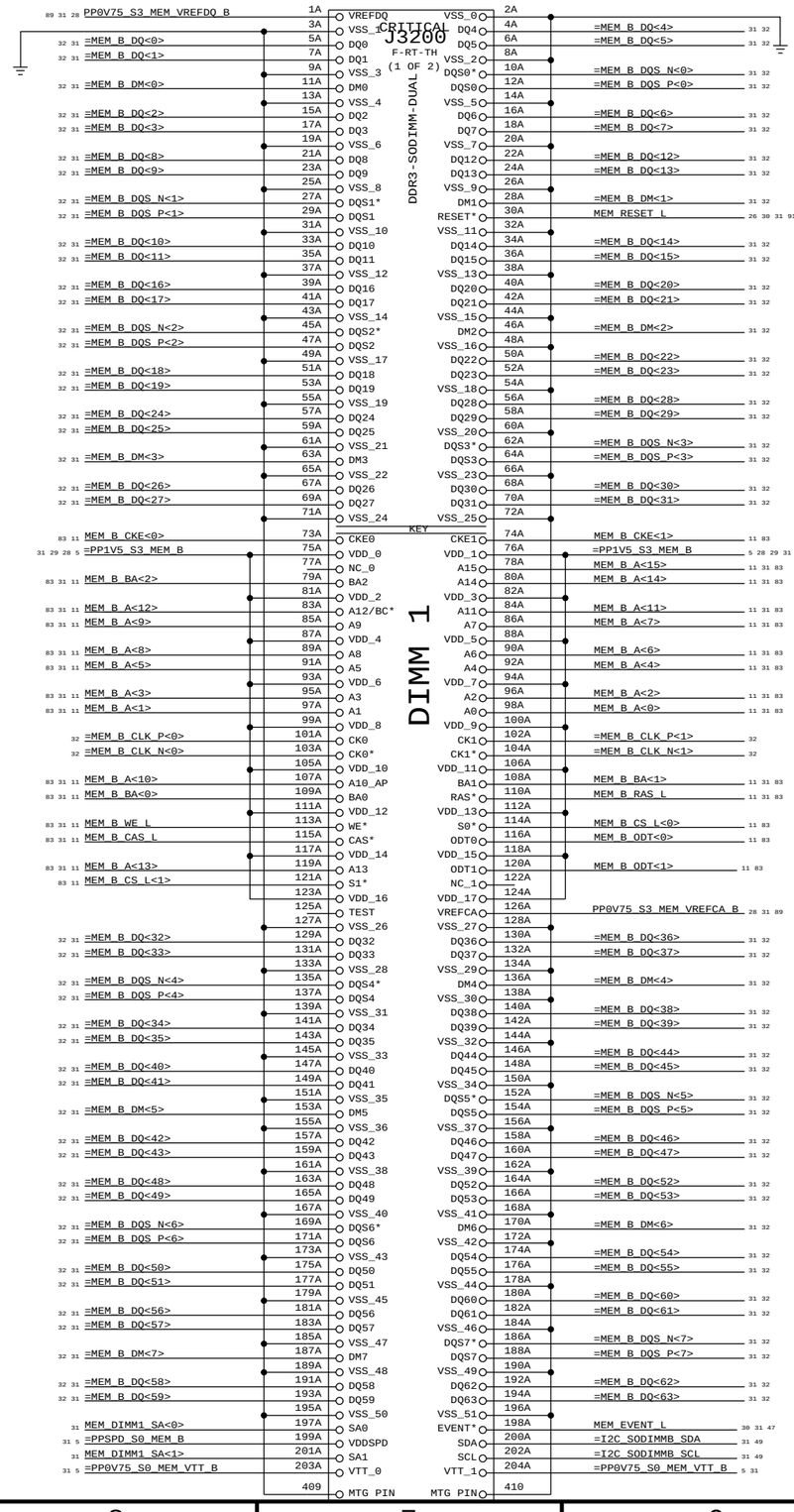
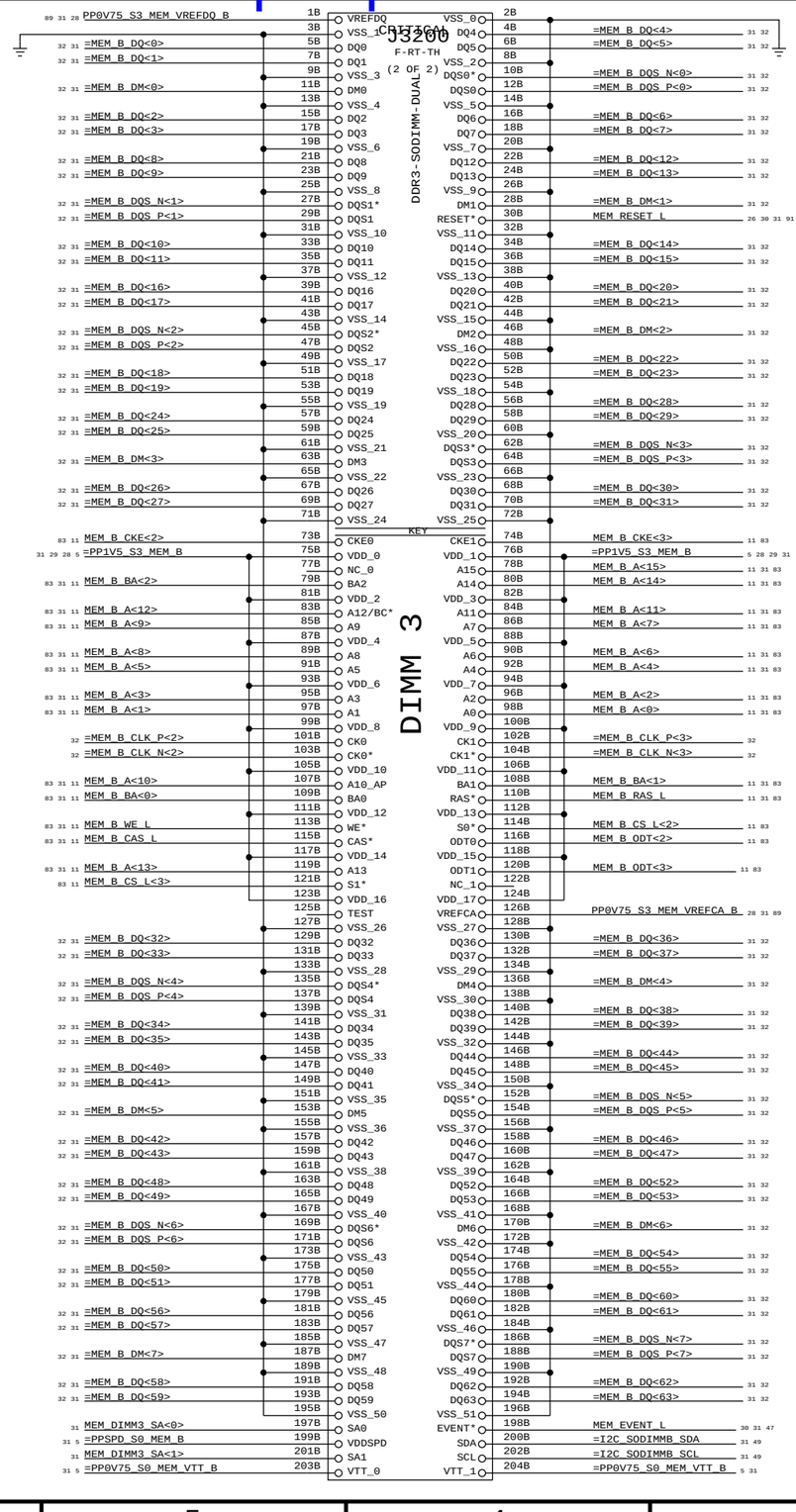
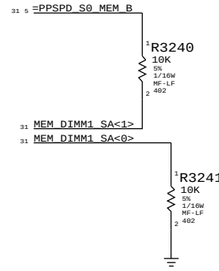
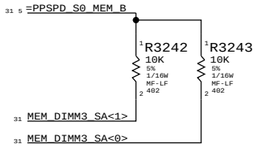


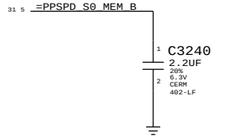


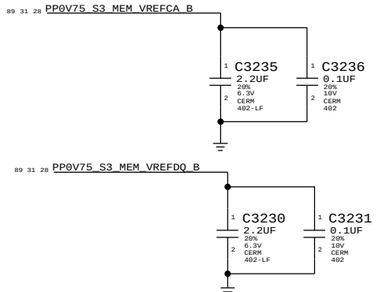
DIMM1 SPD ADDR=0XA4(WR)/0XA5(RD)

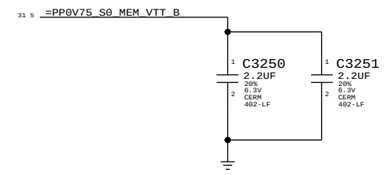


DIMM3 SPD ADDR=0XA6(WR)/0XA7(RD)









Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
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PAGE TITLE
DDR3 SO-DIMM CONNECTOR B

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CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE		=MEM_A_DQS_N<7>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE		=MEM_A_DQS_P<7>
MEM_A_DM<0>	MAKE_BASE=TRUE		=MEM_A_DM<7>
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<60>
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<56>
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<58>
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<59>
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<57>
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<61>
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<62>
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE		=MEM_A_DQS_N<6>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE		=MEM_A_DQS_P<6>
MEM_A_DM<1>	MAKE_BASE=TRUE		=MEM_A_DM<6>
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<49>
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<52>
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<51>
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<50>
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<48>
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<53>
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<55>
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE		=MEM_A_DQS_N<5>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE		=MEM_A_DQS_P<5>
MEM_A_DM<2>	MAKE_BASE=TRUE		=MEM_A_DM<5>
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<40>
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<45>
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<43>
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<42>
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<41>
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<44>
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<46>
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<47>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE		=MEM_A_DQS_N<4>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE		=MEM_A_DQS_P<4>
MEM_A_DM<3>	MAKE_BASE=TRUE		=MEM_A_DM<4>
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<37>
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<33>
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<35>
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<34>
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<36>
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<32>
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<38>
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE		=MEM_A_DQS_N<3>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE		=MEM_A_DQS_P<3>
MEM_A_DM<4>	MAKE_BASE=TRUE		=MEM_A_DM<3>
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<25>
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<29>
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<27>
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<31>
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<28>
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<24>
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<26>
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE		=MEM_A_DQS_N<2>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE		=MEM_A_DQS_P<2>
MEM_A_DM<5>	MAKE_BASE=TRUE		=MEM_A_DM<2>
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<17>
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<16>
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<22>
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<23>
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<21>
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<20>
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<18>
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE		=MEM_A_DQS_N<1>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE		=MEM_A_DQS_P<1>
MEM_A_DM<6>	MAKE_BASE=TRUE		=MEM_A_DM<1>
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<12>
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<13>
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<10>
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<15>
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<8>
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<9>
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<11>
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE		=MEM_A_DQS_N<0>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE		=MEM_A_DQS_P<0>
MEM_A_DM<7>	MAKE_BASE=TRUE		=MEM_A_DM<0>
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<5>
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<4>
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<3>
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<2>
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<1>
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<0>
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<7>
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE		=MEM_B_DQS_N<7>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE		=MEM_B_DQS_P<7>
MEM_B_DM<0>	MAKE_BASE=TRUE		=MEM_B_DM<7>
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<61>
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<60>
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<62>
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<63>
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<56>
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<57>
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<58>
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE		=MEM_B_DQS_N<6>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE		=MEM_B_DQS_P<6>
MEM_B_DM<1>	MAKE_BASE=TRUE		=MEM_B_DM<6>
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<51>
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<54>
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<53>
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<52>
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<48>
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<49>
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<50>
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE		=MEM_B_DQS_N<5>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE		=MEM_B_DQS_P<5>
MEM_B_DM<2>	MAKE_BASE=TRUE		=MEM_B_DM<5>
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<45>
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<40>
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<42>
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<47>
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<44>
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<41>
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<46>
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE		=MEM_B_DQS_N<4>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE		=MEM_B_DQS_P<4>
MEM_B_DM<3>	MAKE_BASE=TRUE		=MEM_B_DM<4>
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<32>
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<39>
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<37>
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<38>
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<35>
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<34>
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<36>
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE		=MEM_B_DQS_N<3>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE		=MEM_B_DQS_P<3>
MEM_B_DM<4>	MAKE_BASE=TRUE		=MEM_B_DM<3>
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<28>
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<24>
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<31>
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<30>
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<29>
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<25>
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<27>
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE		=MEM_B_DQS_N<2>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE		=MEM_B_DQS_P<2>
MEM_B_DM<5>	MAKE_BASE=TRUE		=MEM_B_DM<2>
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<18>
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<20>
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<23>
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<22>
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<19>
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<21>
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<17>
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE		=MEM_B_DQS_N<1>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE		=MEM_B_DQS_P<1>
MEM_B_DM<6>	MAKE_BASE=TRUE		=MEM_B_DM<1>
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<8>
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<14>
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<10>
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<11>
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<9>
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<15>
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<12>
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE		=MEM_B_DQS_N<0>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE		=MEM_B_DQS_P<0>
MEM_B_DM<7>	MAKE_BASE=TRUE		=MEM_B_DM<0>
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<2>
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<1>
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<3>
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<7>
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<4>
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<5>
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<6>
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<0>

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE		=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE		=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE		=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE		=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE		=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE		=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE		=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE		=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>			=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE		=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE		=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE		=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE		=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE		=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE		=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE		=MEM_B_CLK_N<3>

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

DDR3 ALIAS AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D

REVISION A.0.0

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3.3V S3 CURRENT	D0:D2,D3HOT	D3COLD
MAX CONT:	1100MA	100MA
MAX PEAK:	2750MA	2750MA
1.5V CURRENT		
MAX CONT:	N/U	N/U
MAX PEAK:	N/U	N/U

NOTE: CURRENT DATA PER JAN 12,2008 PCIE MINI CEM ECN

NO STUFF
R3400
0
5%
1/16W
MF-LF
402

NO STUFF
R3401
0
5%
1/16W
MF-LF
402

CRITICAL
J3400
AS0B226-S40N-7F
F-RT-SM

516S0457

36 18 OUT PCIE_WAKE_L
RSVD_MINI_WLAN_ACTIVE
RSVD_MINI_BT_ACTIVE
17 14 OUT MINI_CLKREQ_L
84 17 IN PCIE_CLK100M_MINI_N
84 17 IN PCIE_CLK100M_MINI_P

RESERVED
RESERVED

84 17 OUT PCIE_MINI_D2R_N
84 17 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=PLACE CLOSE TO U1800.
C3431
0.1uF
84 17 IN PCIE_MINI_R2D_C_N
10%
16V
X5R
402

PLACEMENT_NOTE=PLACE CLOSE TO U1800.
C3430
0.1uF
84 17 IN PCIE_MINI_R2D_C_P
10%
16V
X5R
402

84 PCIE_MINI_R2D_N
84 PCIE_MINI_R2D_P

MINI_RESET_L
IN 27 91

SMB_MINI_SCL
SMB_MINI_SDA

TP_USB_MININ
TP_USB_MINIP

NO AVAILALBLE USB ON THIS PLATFORM
TARGET CARDS DO NOT USE IT

=PP3V3_S3_MINI 5

C3410 0.1uF 10% 10V CERM 402
C3420 0.1uF 10% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603

=PP1V5_S0_MINI 5

C3400 0.1uF 10% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

R3490 0 =SMB_MINI_SCL 49
R3491 0 =SMB_MINI_SDA 49

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCI-E MiniCard Connector

Apple Inc.

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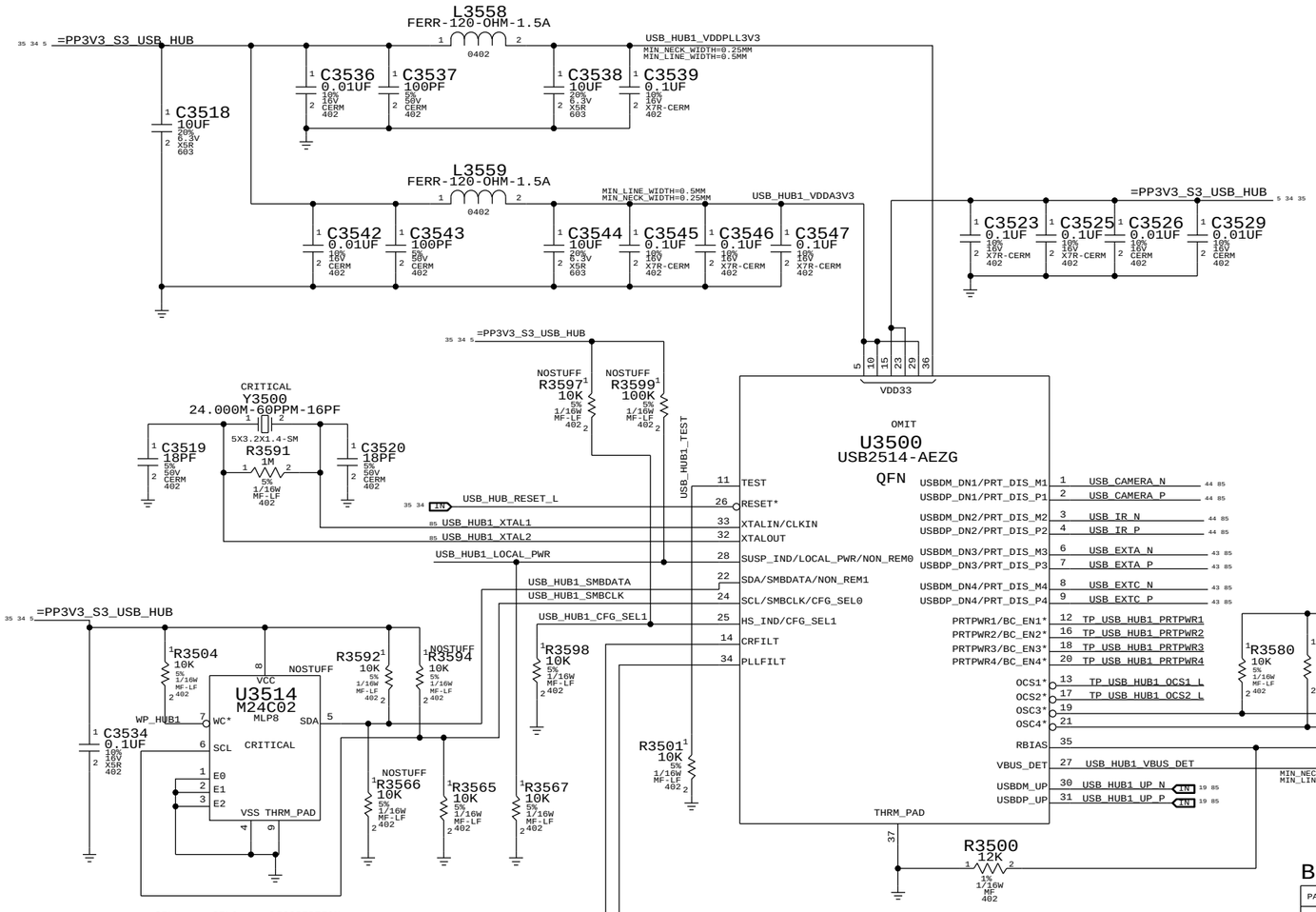
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

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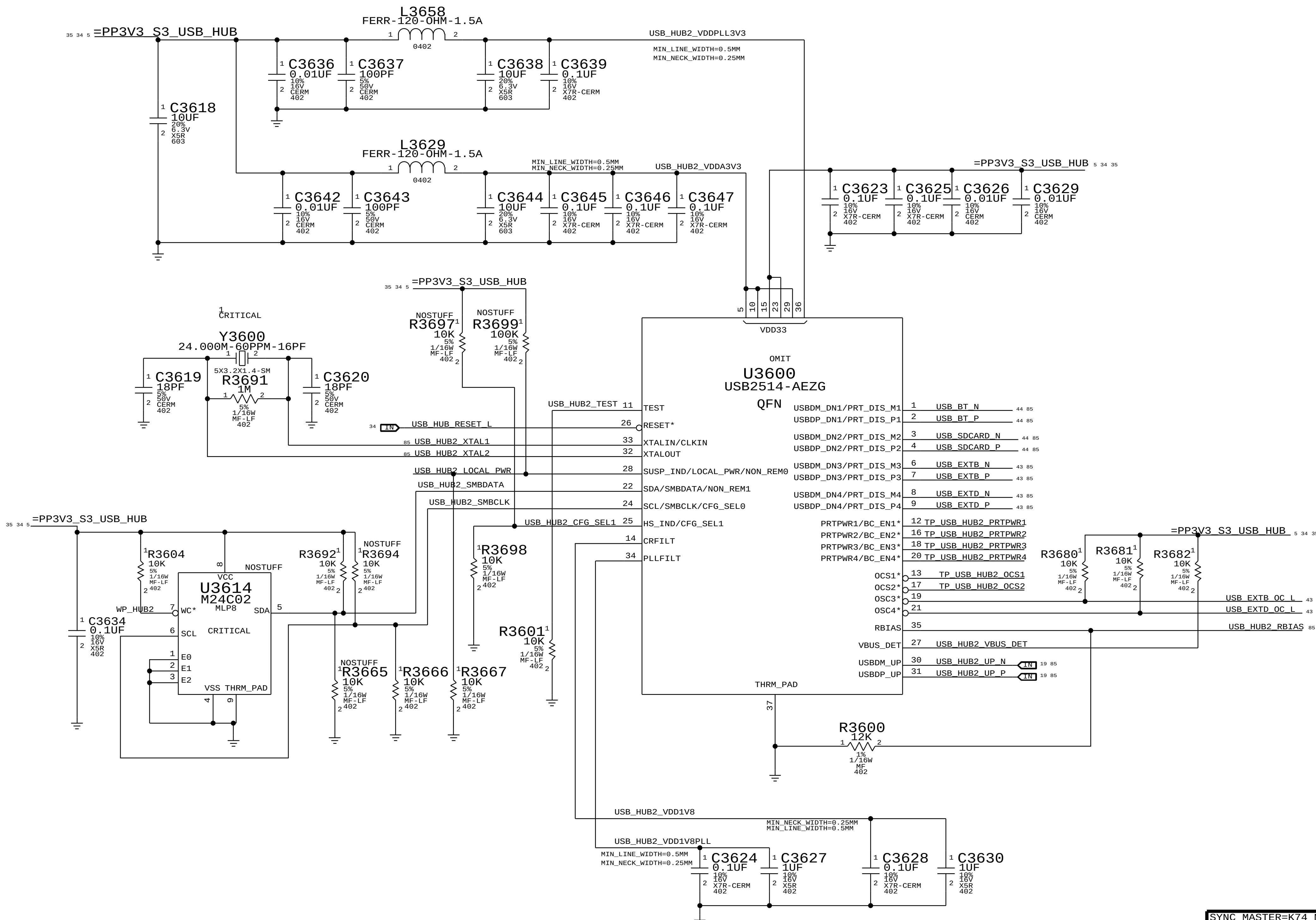
USB HUB-2



SYNC_MASTER=K74_MASTER	SYNC_DATE=N/A
PAGE TITLE	USB HUB 2
DRAWING NUMBER	051-8337
SIZE	D
Apple Inc.	
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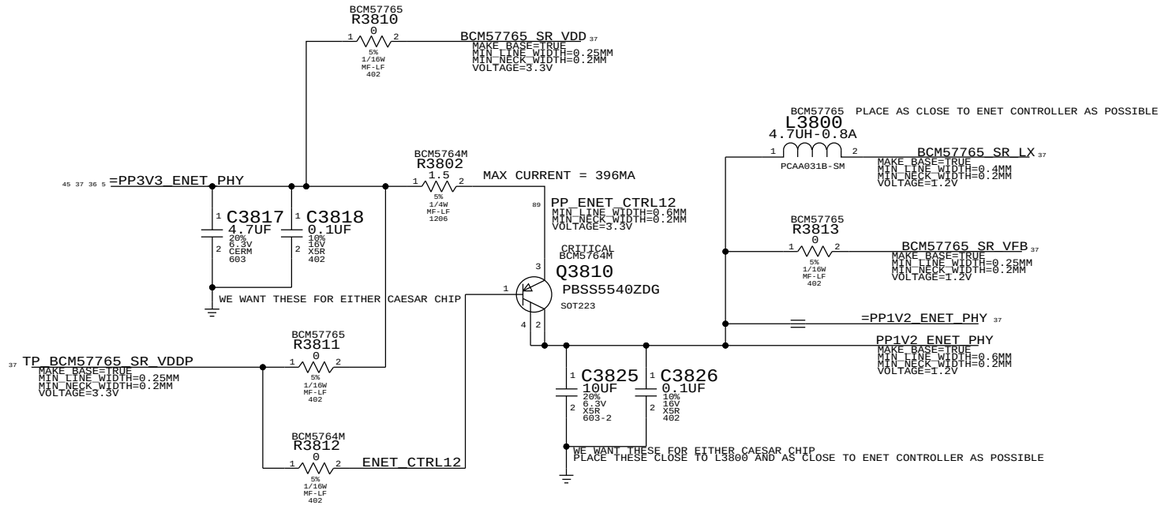
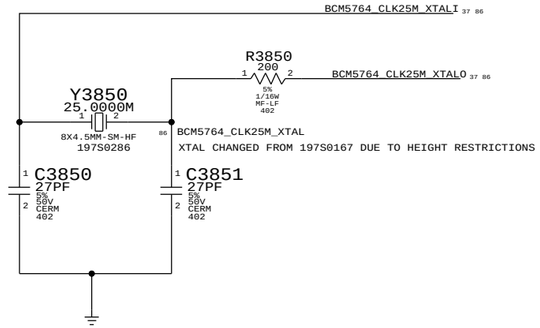
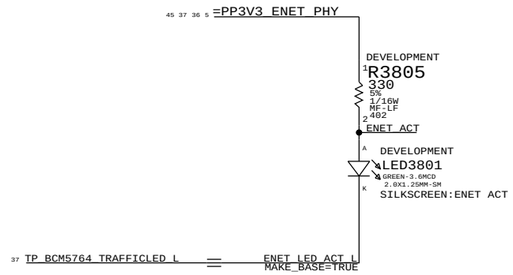
CAESAR II/IV 1V2 RAIL SUPPLY



CAESAR II/IV 25MHZ XTAL

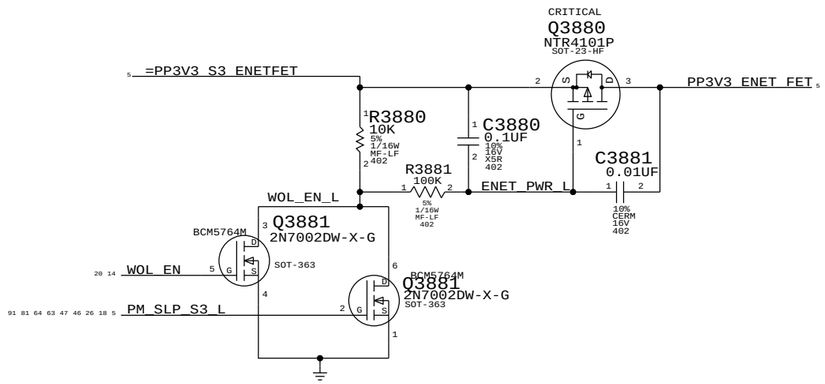


CAESAR II/IV ACTIVITY LED

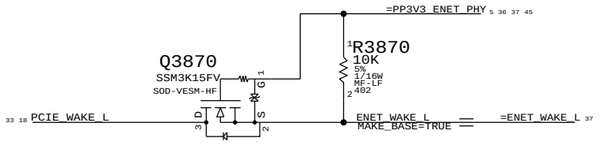


3.3V ENET FET

ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II/IV WAKE# ISOLATION



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Caesar II/IV Support

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

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BCM57765 SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor.

=PP3V3_ENET_PHY
86mA (1000base-T, Caesar II)

PP3V3R1V8_SW_LR_OUT

BCM57765 R3915 0 5% 1/10W MF-LF 402

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDOCR_PIN20 MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765_SR_LX
BCM57765_SR_VFB

BCM57765 R3920 0 5% 1/10W MF-LF 402

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-0.5A SM
PP3V3_ENET_PHY_XTALVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
BCM57765_XTALVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765 R3900 0 5% 1/16W MF-LF 402

C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A SM
PP3V3_ENET_PHY_BIASVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A SM
PP3V3_ENET_PHY_AVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3920 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V

C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

BCM57765 R3940 4.7K 5% 1/10W MF-LF 402
BCM57765 R3941 4.7K 5% 1/10W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

AVDDH BIASVDDH VDDC VDDIO XTALVDDH VDDIO VDDIO VDDC REGCTL12 VDDIO WAKE* AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC VDDC

CRITICAL
OMIT
U3900
BCM5764M
QFN-8X8
VERSION 2

=PP3V3_S0_ENETPHY

BCM57765 R3942 1K 5% 1/16W MF-LF 402

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

BCM57765 R3943 0 5% 1/16W MF-LF 402

=ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

SMB_DATA (IPD-BCM57765)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC

BCM57765 R3965 1.24K 1% 1/16W MF-LF 402

THRM_PAD

BCM57765_SR_DISABLE

If BCM57765 switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

TRD0_P
TRD0_N
TRD1_P
TRD1_N
TRD2_P
TRD2_N
TRD3_P
TRD3_N
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

GPIO1_LR_OUT is not for SD Card power, just decoupling for BCM57765 CR I/Os. Connect only to U3900 pins 9 and 20.

PP3V3R1V8_SW_LR_OUT MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

BCM57765 C3970 4.7UF 10% 6.3V X5R-CERM 603
BCM57765 C3971 0.1UF 10% 16V X7R-CERM 402
BCM57765 C3972 0.1UF 10% 16V X7R-CERM 402

GPIO_0/SERIAL_DO
GPIO_1/SERIAL_DI
GPIO_2
NC
DC0
DC4
DC3
DC2
DC1
NC
VMAIN_PRSNT
VAUX_PRSNT
VDDC
SMB_CLK
ENERGY_DET
DC5
SPD1000LED*

NOTE: "IPx" == Programmable pull-up/down

BCM57765_MEDIA_SENSE
BCM57765_SD_DETECT_L
BCM57765_CR_CMD
BCM57765_CR_DATA<4>
BCM57765_CR_DATA<5>
BCM57765_CR_DATA<6>
BCM57765_CR_DATA<7>
BCM57765_CE_L_MS_INS_L
BCM57765_CR_PWREN
BCM57765_SR_DISABLE

BCM57765 R3972 0 5% 1/16W MF-LF 402
BCM57765 R3973 0 5% 1/16W MF-LF 402
BCM57765 R3974 0 5% 1/16W MF-LF 402 PLACE_NEAR=L3999.1:1 mm
BCM57765 R3975 0 5% 1/16W MF-LF 402
BCM57765 R3976 0 5% 1/16W MF-LF 402
BCM57765 R3977 0 5% 1/16W MF-LF 402
BCM57765 R3978 0 5% 1/16W MF-LF 402

ENET_ENERGY_DET
SDCONN_CD_L
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
SDCONN_WP

BCM57765 R3980 0 5% 1/16W MF-LF 402 (See note)
BCM57765 R3981 0 5% 1/16W MF-LF 402
BCM57765 R3982 1K 5% 1/16W MF-LF 402
BCM57765 R3983 4.7K 5% 1/16W MF-LF 402
BCM57765 R3984 4.7K 5% 1/16W MF-LF 402
BCM57765 R3985 1K 5% 1/16W MF-LF 402
BCM57765 R3986 0 5% 1/16W MF-LF 402
BCM57765 R3987 0 5% 1/16W MF-LF 402
BCM57765 R3988 0 5% 1/16W MF-LF 402
BCM57765 R3989 0 5% 1/16W MF-LF 402
BCM57765 R3998 0 5% 1/16W MF-LF 402
BCM57765 R3999 0 5% 1/16W MF-LF 402

All resistors above BOMOPTIONed BCM57765

BCM57765 supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

=PP3V3_ENET_PHY

U3990
AT45DB011D
SOIC-8S1
OMIT

VCC SCK SI CS* SO WP* RESET* GND

C3990 0.1UF 10% 16V X7R-CERM 402

BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO

NOSTUFF
BCM57765 R3990 4.7K 5% 1/16W MF-LF 402
BCM57765 R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function
60-ENERGY_DET
13-WAKE*
53-VMAIN_PRSNT
59-SMB_CLK
58-SMB_DATA
54-VAUX_PRSNT
16-VDDIO
20-XTALVDDH
55-VDDC
17-VDDC
14-VDDC
06-VDDC
26-PCIE_VDDL

BCM57765_CR_PWREN
BCM57765_SR_VFB
BCM57765_CR_DATA<5>
BCM57765_CE_L_MS_INS_L
BCM57765_VMAIN_PRSNT
BCM57765_CR_DATA<6>
BCM57765_SR_LX
BCM57765_VDDOCR_PIN20
BCM57765_CR_DATA<7>
BCM57765_XTALVDDH
BCM57765_SR_VDD
BCM57765_SMB_CLK
BCM57765_CR_CMD

L3999 FERR-600-OHM-0.5A SM CRITICAL
PLACE_NEAR=U3900.26:2 mm

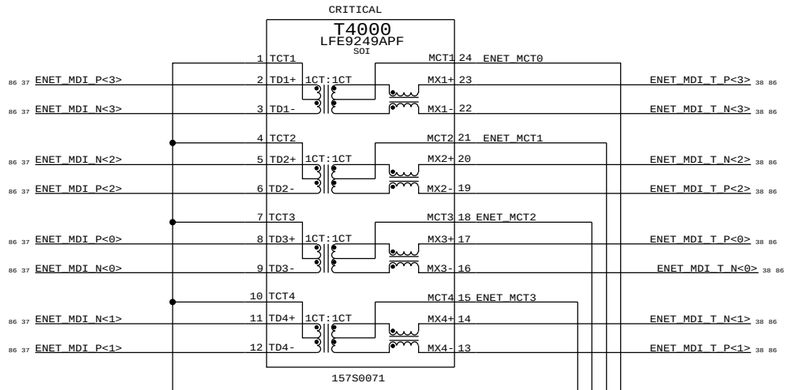
Keep net short, with no stubs.

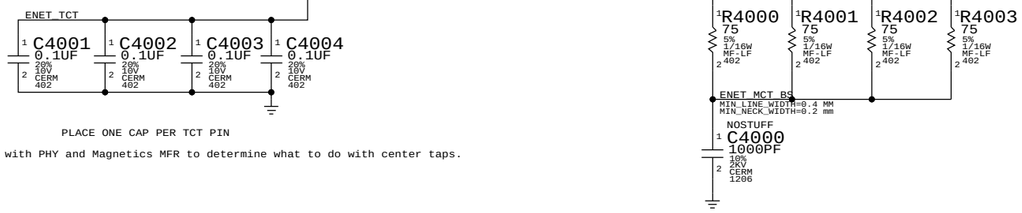
BCM5764M C3999 0.1UF 10% 16V X7R-CERM 402 PLACE_NEAR=U3900.26:1 mm
BCM5764M C3998 4.7UF 10% 6.3V X5R-CERM 603 PLACE_NEAR=L3999.1:1 mm

SYNC_MASTER=T27 SYNC_DATE=11/30/2005
PAGE TITLE: Ethernet PHY (Caesar II/IV)

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
PAGE 39 OF 110
SHEET 37 OF 92



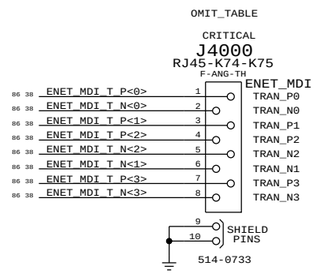


PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.

OMIT_TABLE



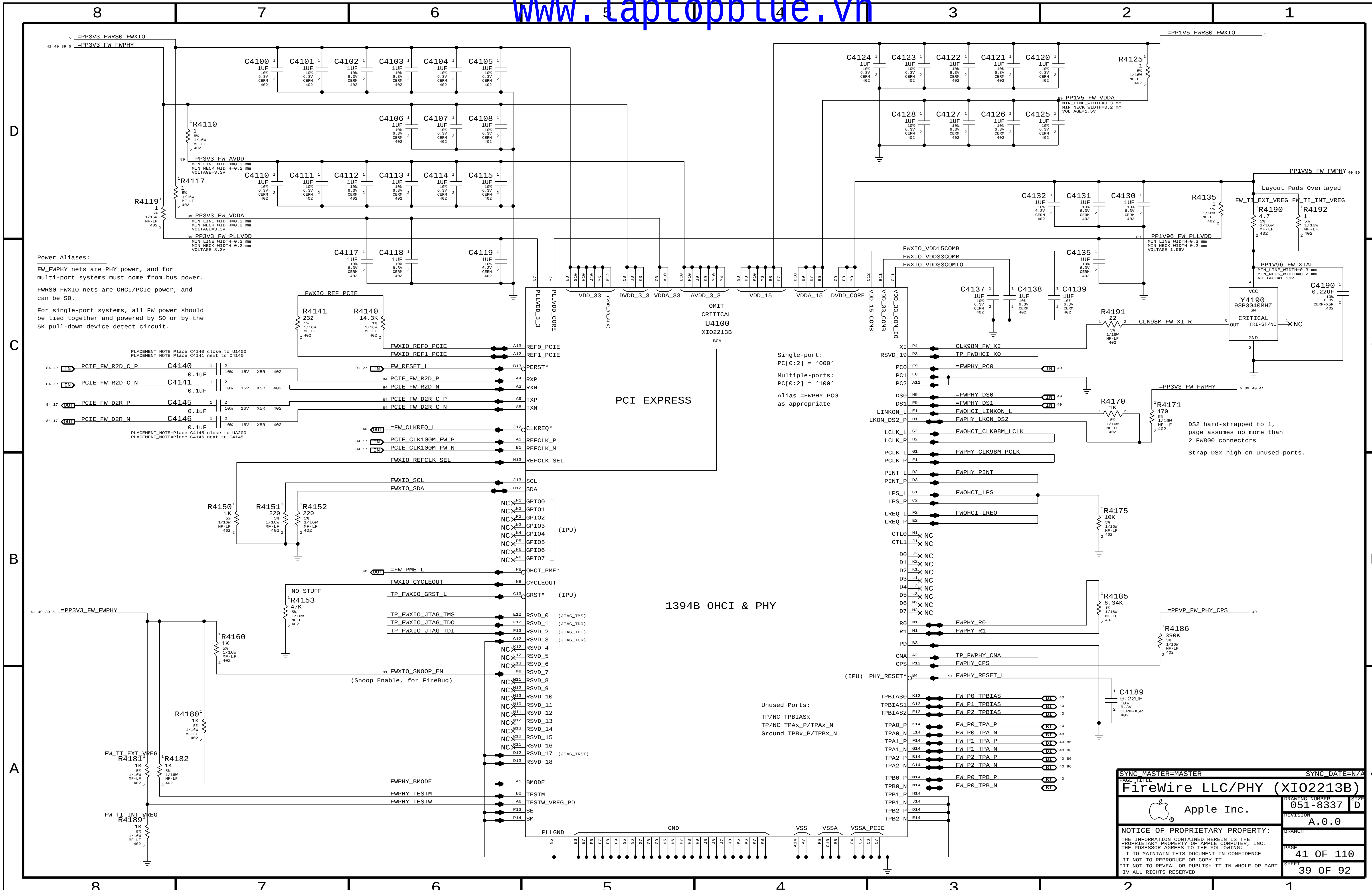
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0654	1	K22/K23 PROD. RJ45	J4000	CRITICAL	METAL_IO
514-0733	1	K74/K75 RJ45, PLASTIC, PD/NI	J4000	CRITICAL	PLASTIC_IO

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
Ethernet Connector

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
PAGE 40 OF 110
SHEET 38 OF 92


Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.
PLACEMENT_NOTE=Place C4140 close to U1400
PLACEMENT_NOTE=Place C4141 next to C4140
PLACEMENT_NOTE=Place C4145 close to UA200
PLACEMENT_NOTE=Place C4146 next to C4145
PCI EXPRESS
1394B OHCI & PHY
OMIT
CRITICAL
U4100
XIO2213B
BGA
Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0 as appropriate
Layout Pads Overlayed
DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors
Strap DSx high on unused ports.
Unused Ports:
TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N
(Snoop Enable, for FireBug)
NO STUFF
Y4190
98P3040MHZ
CRITICAL
SYNC_MASTER=MASTER
SYNC_DATE=N/A
FireWire LLC/PHY (XIO2213B)
Apple Inc.
DRAWING NUMBER 051-8337
SIZE D
REVISION A.0.0
NOTICE OF PROPRIETARY PROPERTY:
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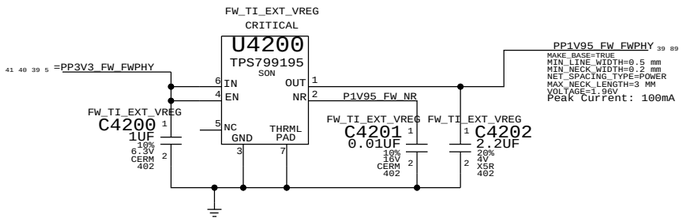
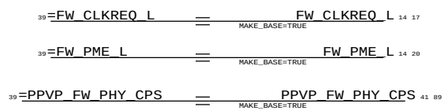
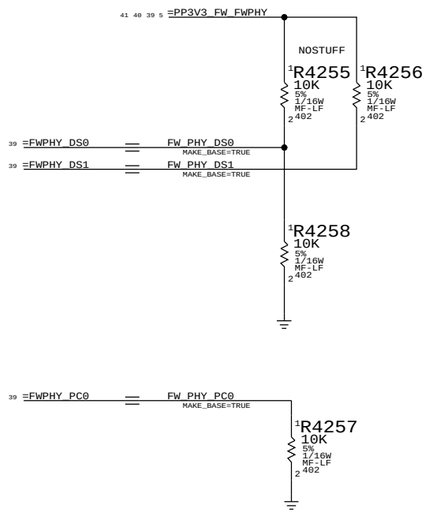
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



1394 PHY STRAPPING OPTIONS

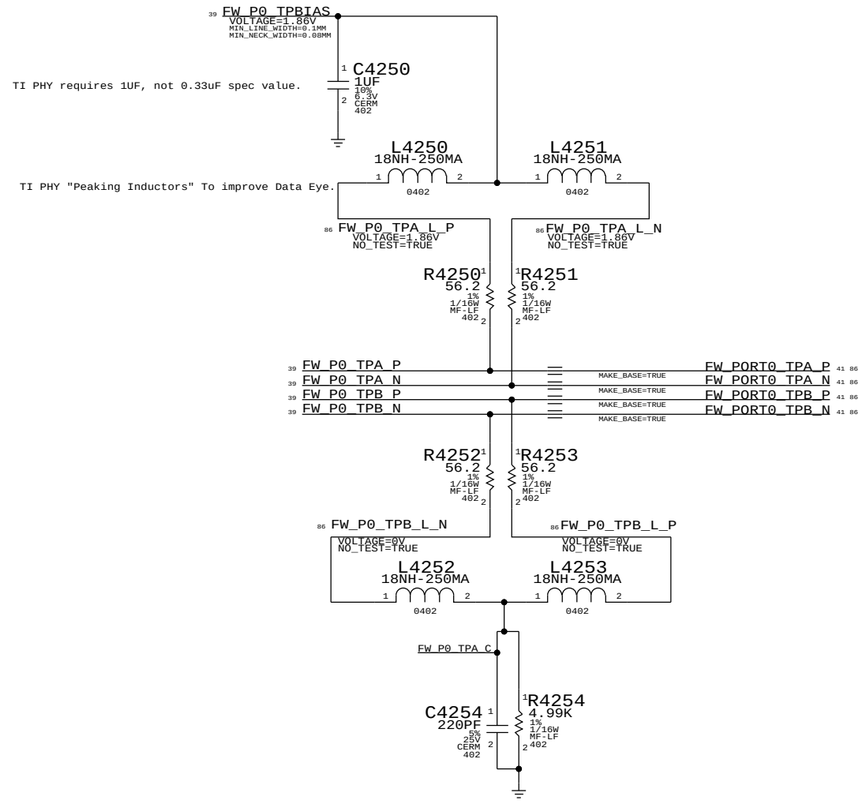


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

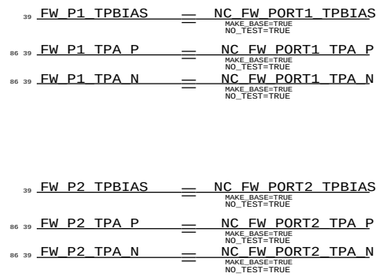
iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: FW: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 42 OF 110

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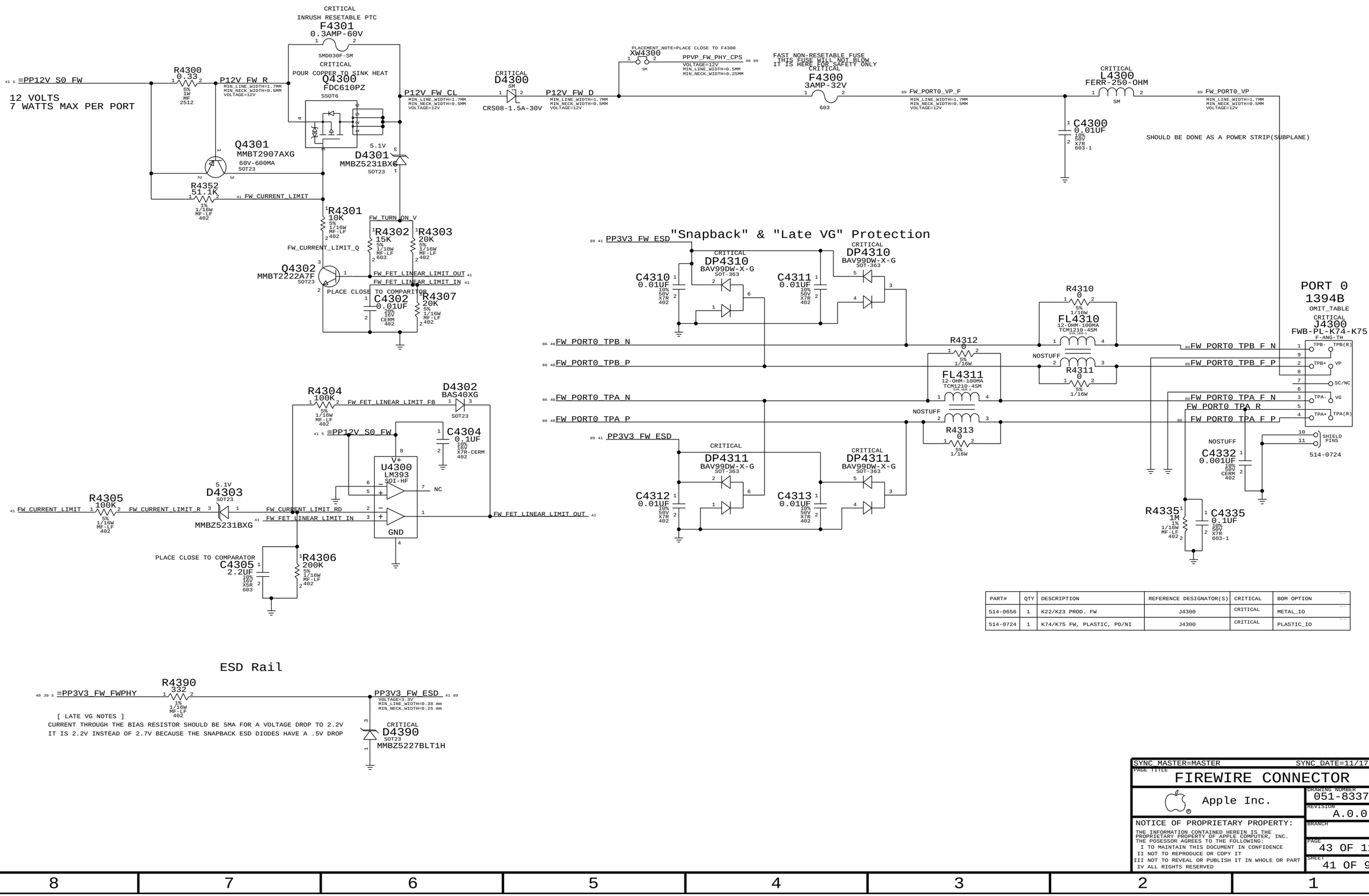

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0656	1	K22/K23 PROD. FW	J4300	CRITICAL	METAL_IO
514-0724	1	K74/K75 FW, PLASTIC, PD/NI	J4300	CRITICAL	PLASTIC_IO

SYNC_MASTER=MASTER SYNC_DATE=11/17/2009

PAGE TITLE: FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 43 OF 110
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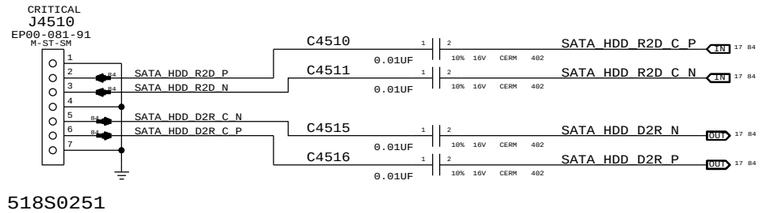
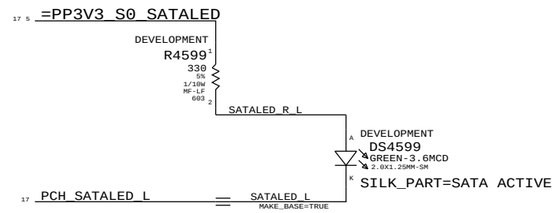
SATA PORT A0 FOR HDD

SILKSCREEN:HDD

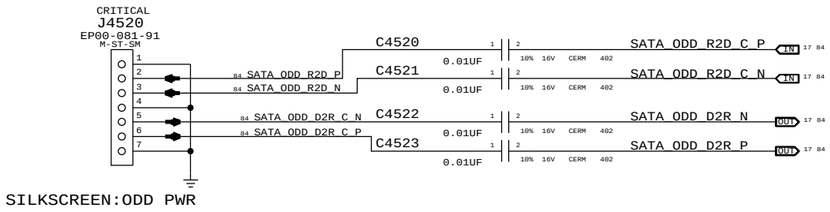


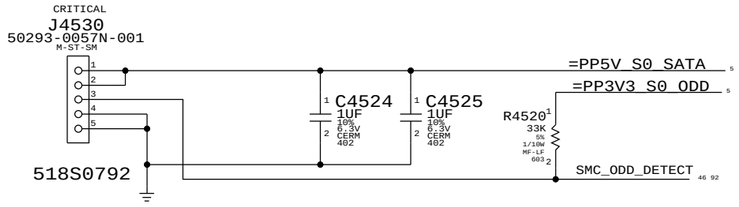
SATA Activity LED



SATA PORT A1 FOR SLIMLINE ODD

SILKSCREEN:ODD





SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
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SHEET: 42 OF 92

USB/SMC DEBUG MUX

=PP3V3_G3H_SMCUSBMUX

C4650 0.1UF 20% 10V CERM 402

U4650 MOJOMUX PI3USB102ZLE TQFN

SMC_RX_L, SMC_TX_L

USB_EXTD_P, USB_EXTD_N

USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB

R4651 0 PRODUCTION

R4652 0 PRODUCTION

PORT 3

=PP5V_S3_USB

U4601 TPS2060 MSOP

USB_EXTC_OC_L, USB_EXTD_OC_L

R4600 10K 5% 1/16W MF-LF 402

USB_PWR_ENA_L

Q4600 2N7002 SOT23-HF1

PM_EN_USB_PWR

C4605 0.1UF 20% 10V CERM 402

C4606 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C4621 0.1UF 20% 10V CERM 402

C4631 0.1UF 20% 10V CERM 402

L4630 FERR-250-OHM SM

C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

USB_D_MUXED_N, USB_D_MUXED_P

L4631 120-OHM-90MA DLP0NS

USB_PORT3_N, USB_PORT3_P

J4630 USB-MG4-K74-K75 F-ANG-TH

VDD, D-, D+, GND, VBUS, DATA-, DATA+, GND

514-0732

D4630 RCLAMP0502N SLP1210N6

PORT 2

U4600 TPS2060 MSOP

=PP5V_S3_USB

USB_EXTA_OC_L, USB_EXTB_OC_L

C4601 0.1UF 20% 10V CERM 402

C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C4603 0.1UF 20% 10V CERM 402

C4611 0.1UF 20% 10V CERM 402

L4610 FERR-250-OHM SM

C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

L4611 120-OHM-90MA DLP0NS

USB_EXTB_N, USB_EXTB_P

USB_PORT1_N, USB_PORT1_P

J4610 USB-MG6-K74-K75 F-ANG-TH

514-0731

D4610 RCLAMP0502N SLP1210N6

L4620 FERR-250-OHM SM

C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

L4621 120-OHM-90MA DLP0NS

USB_EXTC_N, USB_EXTC_P

USB_PORT2_N, USB_PORT2_P

J4620 USB-MG4-K74-K75 F-ANG-TH

514-0732

D4620 RCLAMP0502N SLP1210N6

PORT 1

L4600 FERR-250-OHM SM

C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

L4601 120-OHM-90MA DLP0NS

USB_EXTA_N, USB_EXTA_P

USB_PORT0_N, USB_PORT0_P

J4600 USB-MG6-K74-K75 F-ANG-TH

514-0731

D4600 RCLAMP0502N SLP1210N6

PORT 0

USB PORT POWER:

EACH PORT IS HARDWARE CAPABLE OF 1.5A
SOFTWARE WILL ALLOW 500 MA PER PORT, PLUS
  1200 MA 'EXTRA' POWER TO BE DISTRIBUTED TO APPROVED
  DEVICES ON A FIRST-COME, FIRST-SERVED BASIS

EXAMPLE: WIRED KEYBOARD WITH 2 500 MA PORTS = 1100 MA TOTAL ON ONE PORT
   500 MA STANDARD + 600 MA 'EXTRA' POWER
IPHONE 'FAST' CHARGING AT 1000 MA ON ANOTHER PORT
   500 MA STANDARD + 500 MA 'EXTRA' POWER
2 STANDARD PORTS AT 500 MA EACH
TOTAL: 3100 MA (STILL 100 MA SPARE EXTRA POWER)

IN S3, SOFTWARE MAY ALLOCATE UP TO 2000 MA TOTAL FOR CHARGING DEVICES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0672	2	K22/K23 PROD. USB	J4600,J4610	CRITICAL	METAL_IO
514-0731	2	K74/K75 USB, PLASTIC, PD/NI	J4600,J4610	CRITICAL	PLASTIC_IO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0659	2	K22/K23 PROD. USB	J4620,J4630	CRITICAL	METAL_IO
514-0732	2	K74/K75 USB, PLASTIC, PD/NI	J4620,J4630	CRITICAL	PLASTIC_IO

SYNC_MASTER=MASTER SYNC_DATE=11/30/2009

PAGE TITLE: EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 46 OF 110
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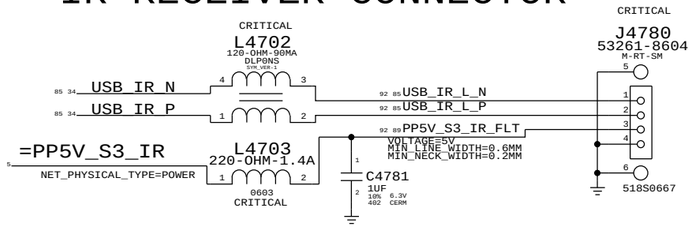
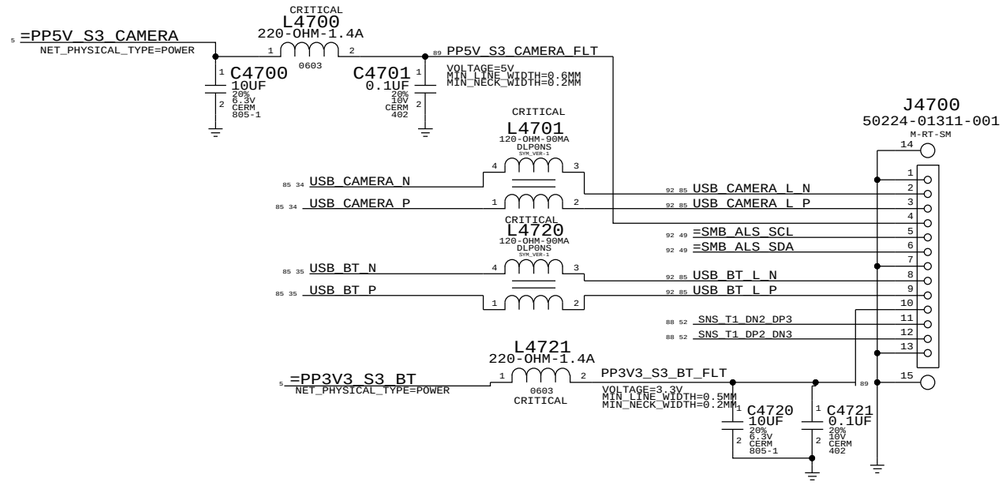
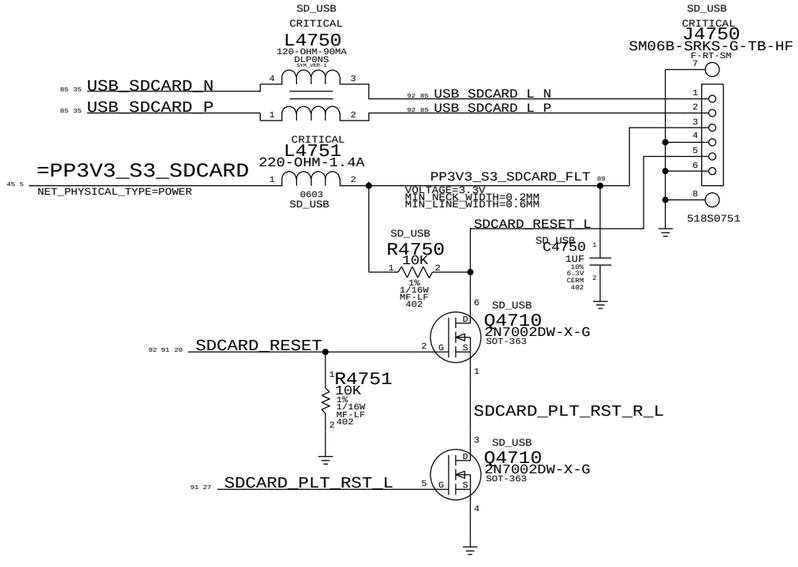
IR RECEIVER CONNECTOR



CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



LAZAURS SD CARD READER BOARD CONNECTOR
BACKUP TO CAESAR IV



SYNC_MASTER=MASTER	SYNC_DATE=11/06/2009
PAGE TITLE: Internal USB Connections	
Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 47 OF 110
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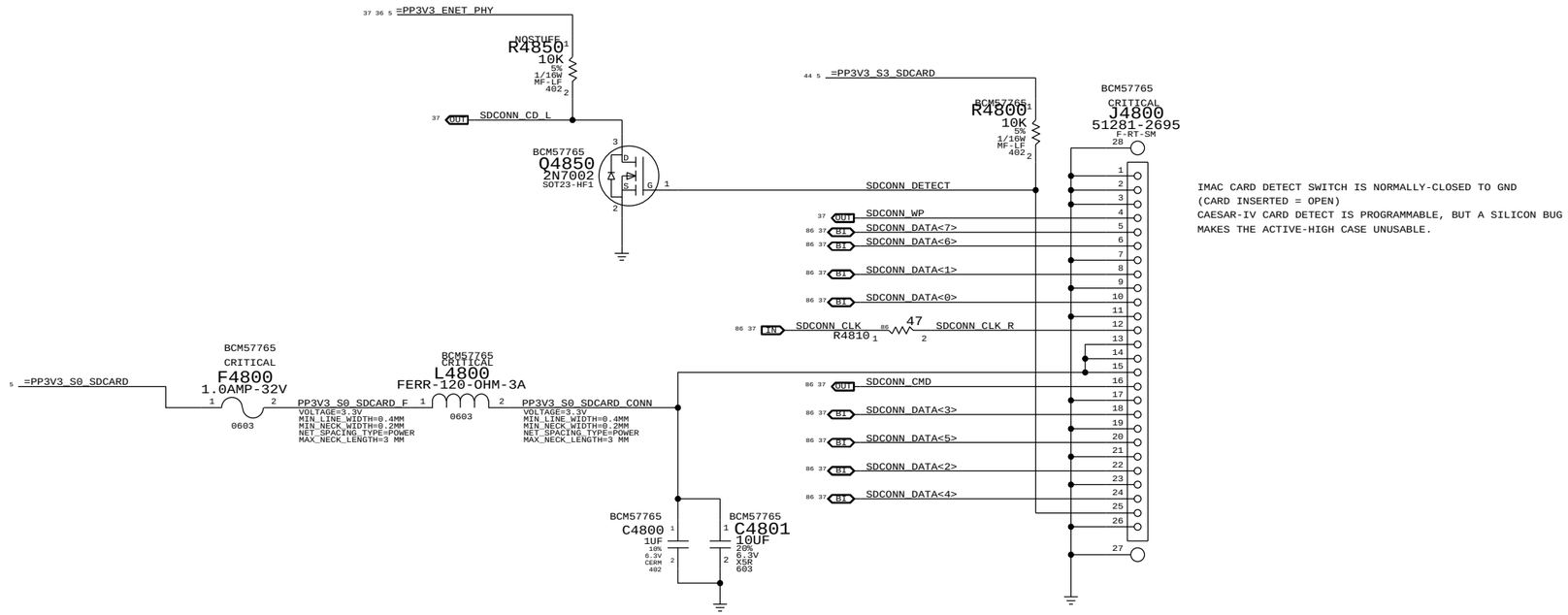

IMAC CARD DETECT SWITCH IS NORMALLY-CLOSED TO GND
(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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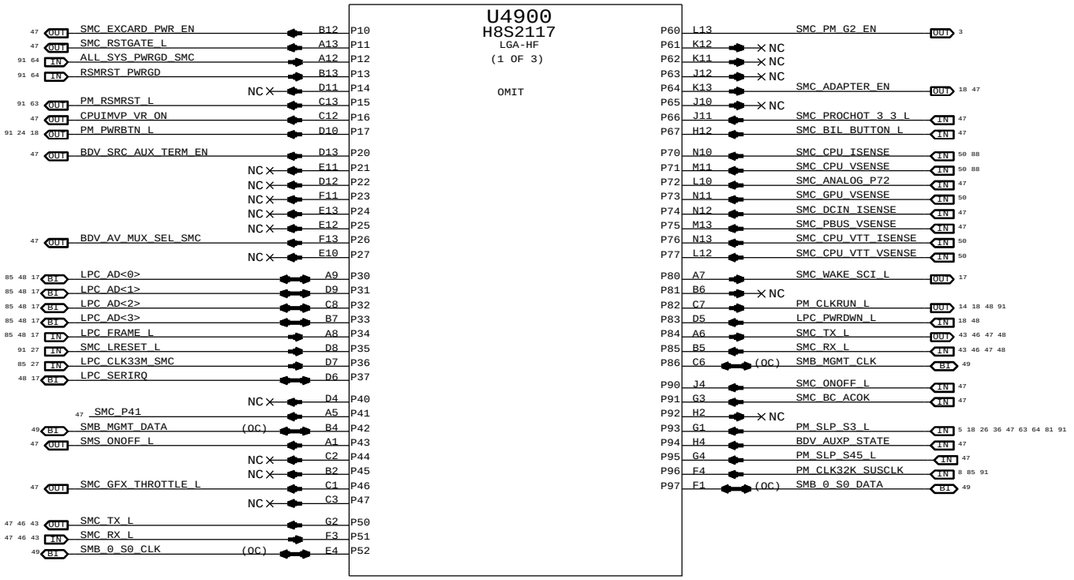
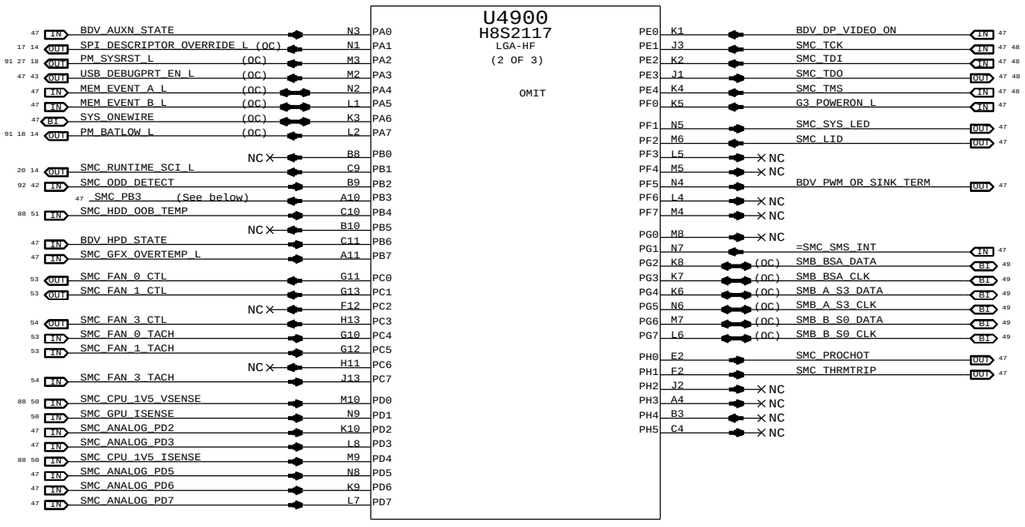
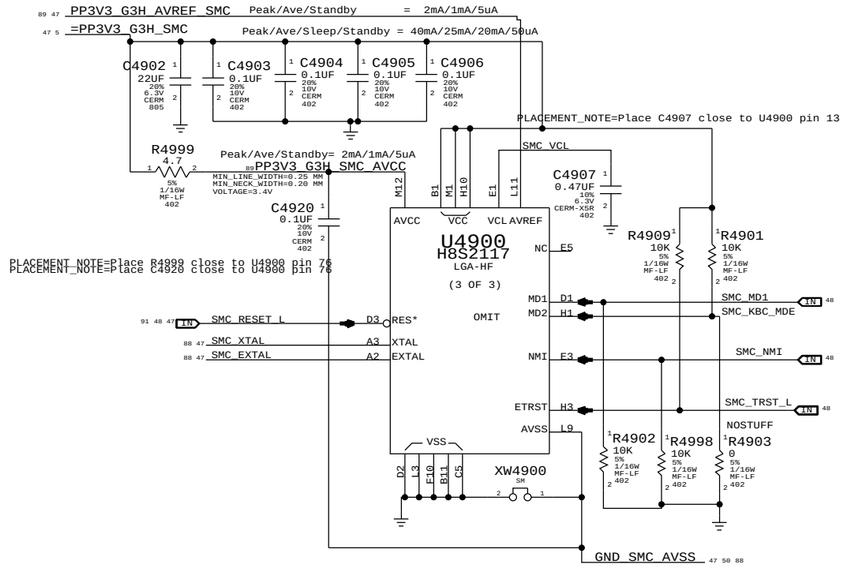
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
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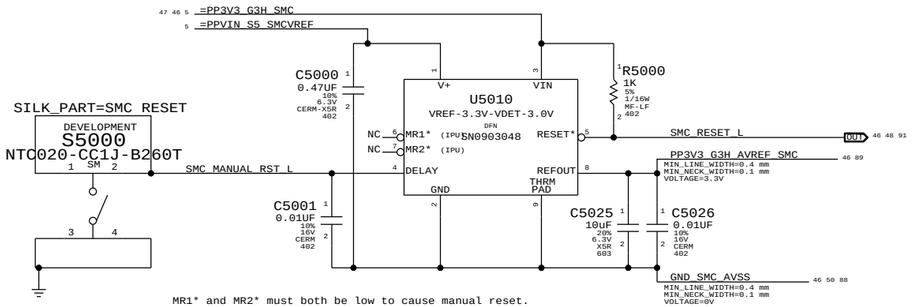
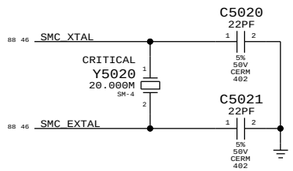
SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

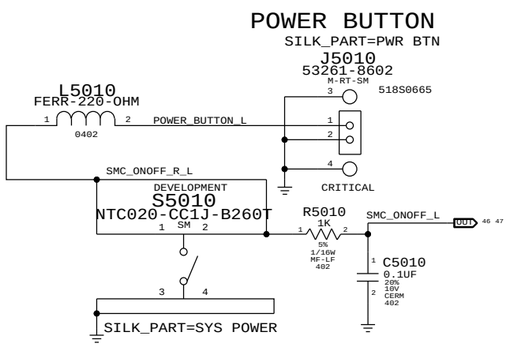
NOTE: Internal pull-ups are to VIN, not V+.

SMC Crystal Circuit

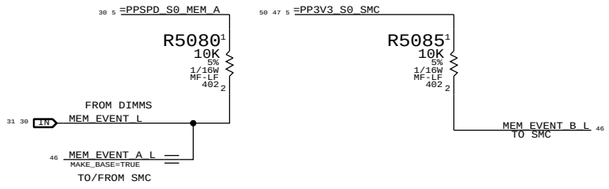


POWER BUTTON

SILK_PART=PWR BTN



MEM_EVENT



MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L — MXM_ALERT_L (MAKE_BASE=TRUE)
SMC_GFX_THROTTLE_L — MXM_PWR_LEVEL (MAKE_BASE=TRUE)
CPUIMVP_VR_ON — SMC_DELAYED_PWRGD (MAKE_BASE=TRUE)

UNUSED PORT 7 ANALOG SENSORS

SMC_ANALOG_P72
SMC_DCIN_ISENSE
SMC_PBUS_VSENSE
SMC_UNUSED_ADC_PORT7 (MAKE_BASE=TRUE)
R5002 10K 5% 1/16W MF-LF 402

UNUSED PORT D ANALOG (INTERNAL PULLUPS)

SMC_ANALOG_PD2 — NC_SMC_ANALOG_PD2 (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_ANALOG_PD3 — NC_SMC_ANALOG_PD3 (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_ANALOG_PD5 — NC_SMC_ANALOG_PD5 (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_ANALOG_PD6 — NC_SMC_ANALOG_PD6 (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_ANALOG_PD7 — NC_SMC_ANALOG_PD7 (MAKE_BASE=TRUE, NO_TEST=TRUE)

UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
SMS_ONOFF_L — TP_SMS_ONOFF_L
SMC_RSTGATE_L — TP_SMC_RSTGATE_L
SMC_P41 — TP_SMC_P41
SMC_SYS_LED — TP_SMC_SYS_LED
SMC_PB3 — TP_SMC_PB3
(MAKE_BASE=TRUE)

BDV_PWM_OR_SINK_TERM — TP_BDV_PWM_OR_SINK_TERM
BDV_SRC_AUX_TERM_EN — TP_BDV_SRC_AUX_TERM_EN
BDV_AV_MUX_SEL_SMC — TP_BDV_AV_MUX_SEL_SMC
(MAKE_BASE=TRUE)

TIES OFF AUDIO DETECT CIRCUIT WHEN BIDIVI IS NOT USED

BDV_AV_MUX_SEL — GND_AUDIO_CODEC (MAKE_BASE=TRUE)

=PP3V3_G3H_SMC

SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402	
SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402	
SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402	
SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402	
SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402	
SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402	
SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402	
SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402	
SMC_BIL_BUTTON_L	R5092	10K	5%	1/16W	MF-LF	402	
SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402	
SMC_ADAPTER_EN	R5049	10K	5%	1/16W	MF-LF	402	
USB_DEBUGPRT_EN_L	R5098	10K	5%	1/16W	MF-LF	402	
=SMC_SMS_INT — SMC_SMS_INT (MAKE_BASE=TRUE)	R5091	10K	5%	1/16W	MF-LF	402	
SMC_LID	R5087	10K	5%	1/16W	MF-LF	402	
G3_POWERON_L	R5086	10K	5%	1/16W	MF-LF	402	
BDV_AUXP_STATE	R5060	100K	5%	1/16W	MF-LF	402	
BDV_AUXN_STATE	R5061	100K	5%	1/16W	MF-LF	402	
BDV_HPD_STATE	R5062	100K	5%	1/16W	MF-LF	402	

=PP3V3_S0_SMC

SMC_GFX_OVERTEMP_L	R5099	10K	5%	1/16W	MF-LF	402	

BDV_DP_VIDEO_ON	R5063	100K	5%	1/16W	MF-LF	402	
PM_SLP_S3_L	R5094	100K	5%	1/16W	MF-LF	402	
PM_SLP_S5_L	R5090	100K	5%	1/16W	MF-LF	402	
PM_SLP_S4_L	R5089	100K	5%	1/16W	MF-LF	402	
PM_SLP_S45_L							

SMC PROCHOT 3.3V LEVEL SHIFTING

=PP3V3_S0_SMC_LS
=PPVTT_S0_CPU
R5078 470 5% 1/10W MF-LF 402
R5070 3.3K 5% 1/16W MF-LF 402
TO SMC
SMC_PROCHOT_3_3_L
TO CPU
CPU_PROCHOT_L
R5071 3.3K 5% 1/16W MF-LF 402
CPU_PROCHOT_L_R
CPU_PROCHOT_BUF
Q5077 MMDT3904-X-G SOT-363-LF
SMC_PROCHOT
FROM SMC
Q5095 2N7002DW-X-G SOT-363

SMC & MXM THERMTRIP LEVEL SHIFTING

=PP3V3_S0_SMC_LS
MXM
R5018 0 5% 1/16W MF-LF 402
PM_THRMTRIP_L
PULL-UP ON PAGE 14
R5068 10K 5% 1/16W MF-LF 402
R5069 3.3K 5% 1/16W MF-LF 402
MXM_THRMTRIP_L
MXM_THRMTRIP
Q5096 2N7002DW-X-G SOT-363
Q5095 2N7002DW-X-G SOT-363
MXM_OVERT_L
FROM MXM
SMC_THRMTRIP
FROM SMC

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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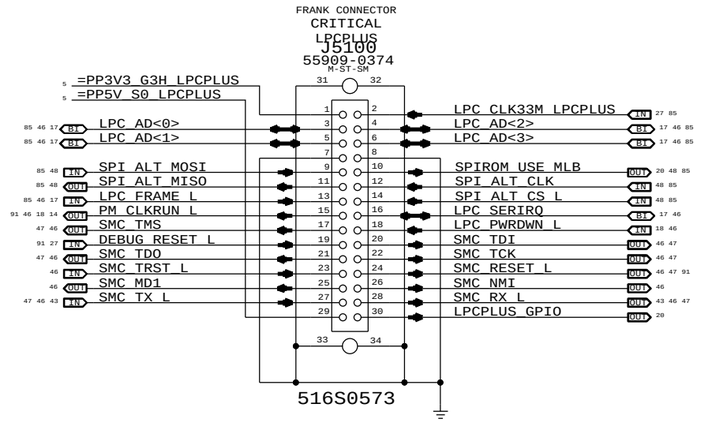
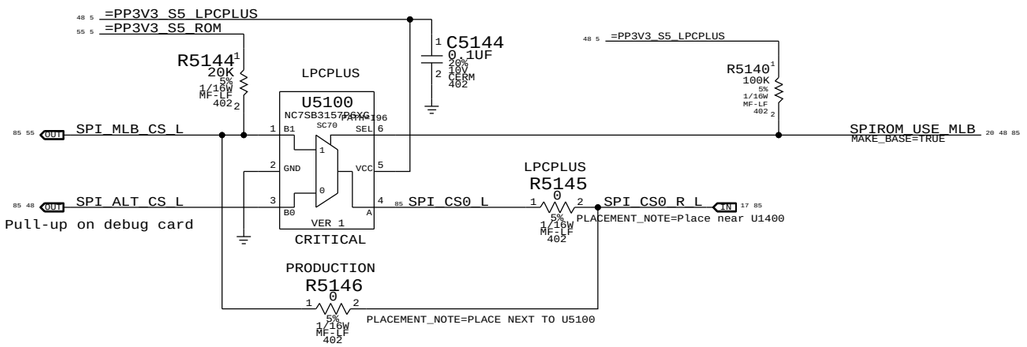
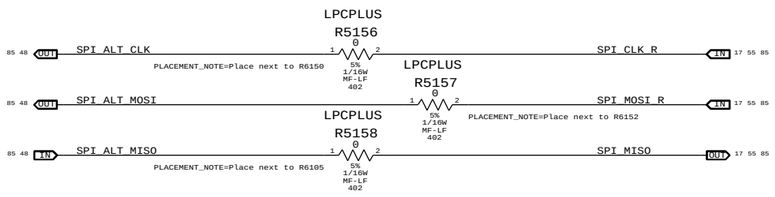
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
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PCH "SMBUS" CONNECTIONS

49 5 =PP3V3_S0_SMBUS

R5208 1 2.2K 5% 1/16W MF-LF 402 2
R5209 1 2.2K 5% 1/16W MF-LF 402 2

PCH
U1800
(MASTER)

88 17 SMBUS_PCH_CLK MAKE_BASE=TRUE
88 17 SMBUS_PCH_DATA MAKE_BASE=TRUE

MEMORY A DIMMS
J3100-A/B
(Write: 0xA0 Read: 0xA1)
(WRITE: 0XA2 READ: 0XA5)
=I2C_SODIMMA_SCL 30
=I2C_SODIMMA_SDA 30

MEMORY B DIMMS
J3200-A/B
(WRITE: 0XA4 READ: 0XA3)
(WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL 31
=I2C_SODIMMB_SDA 31

MIKEY
U6806
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL 62
=I2C_AUDIO_SDA 62

XDP
J2500
(MASTER)

24 =SMBUS_XDP_SCL
24 =SMBUS_XDP_SDA

CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL 25
=SMBUS_CK505_SDA 25

MEMORY VREF DAC
U2900
(WRITE: 0X98 READ: 0X99)
=I2C_VREFDACS_SCL 28
=I2C_VREFDACS_SDA 28

MEMORY VREF MARGIN
U2910
(WRITE: 0X30 READ: 0X31)
=I2C_PCA9557D_SCL 28
=I2C_PCA9557D_SDA 28

PCH "SML 1" CONNECTIONS

49 5 =PP3V3_S0_SMBUS

NOSTUFF R5204 1 8.2K 5% 1/16W MF-LF 402 2
NOSTUFF R5205 1 8.2K 5% 1/16W MF-LF 402 2

R5206 0 5% 1/16W MF-LF 402 1 2
R5207 0 5% 1/16W MF-LF 402 1 2

PCH
U1800
(SLAVE)
(WRITE: 0X88 READ: 0X89)

88 17 SML_PCH_1_CLK MAKE_BASE=TRUE
88 17 SML_PCH_1_DATA MAKE_BASE=TRUE

PCH "SML 0" CONNECTIONS

49 5 =PP3V3_S0_SMBUS

R5202 1 8.2K 5% 1/16W MF-LF 402 2
R5203 1 8.2K 5% 1/16W MF-LF 402 2

PCH
U1800
(MASTER)

88 17 SML_PCH_0_CLK MAKE_BASE=TRUE
88 17 SML_PCH_0_DATA MAKE_BASE=TRUE

SMC "B" SMBus Connections

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 0

5 =PP3V3_S0_SMBUS_SMC_B_S0

R5260 1 2.2K 5% 1/16W MF-LF 402 2
R5261 1 2.2K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)

46 SMB_B_S0_CLK
46 SMB_B_S0_DATA
88 SMBUS_SMC_B_S0_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_B_S0_SDA MAKE_BASE=TRUE

AC/DC PS TEMPS
EMC1403-[1,2]: ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
=SMB_ACDC_SCL 5
=SMB_ACDC_SDA 5

AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81))
OUTPUT VOLTAGE, CURRENT, POWER

SMC "0" SMBus Connections

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

5 =PP3V3_S0_SMBUS_SMC_0_S0

R5250 1 4.7K 5% 1/16W MF-LF 402 2
R5251 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)

46 SMB_0_S0_CLK
46 SMB_0_S0_DATA
88 SMBUS_SMC_0_S0_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_0_S0_SDA MAKE_BASE=TRUE

Also reserve 0x56 and 0x32 per spec

MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
MXM CARD (WRITE: 0X98 READ: 0X99)
=SMB_MXM_THRM_SCL 75
=SMB_MXM_THRM_SDA 75

HEATSINK TEMPS
EMC1414: U5500
(WRITE: 0XD8 READ: 0XD9)
=SMB_SNS1_SCL 52
=SMB_SNS1_SDA 52

AMB,ODD,SKIN TEMPS
TMP423: U5550
(WRITE: 0X9A READ: 0X9B)
=SMB_SNS2_SCL 52
=SMB_SNS2_SDA 52

PCIE MINI-CARD X18 WI-FI MODULE
TMP106: J3400
(WRITE: 0X90 READ: 0X91)
=SMB_MINI_SCL 33
=SMB_MINI_SDA 33

SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

5 =PP3V3_S3_SMBUS_SMC_A_S3

R5270 1 4.7K 5% 1/16W MF-LF 402 2
R5271 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)

46 SMB_A_S3_CLK
46 SMB_A_S3_DATA
88 SMBUS_SMC_A_S3_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_A_S3_SDA MAKE_BASE=TRUE

ALS
(WRITE: 0X52 READ: 0X53)
=SMB_ALS_SCL 44 92
=SMB_ALS_SDA 44 92

SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY

5 =PP3V3_S0_SMBUS_SMC_BSA

R5280 1 4.7K 5% 1/16W MF-LF 402 2
R5281 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(SLAVE)

46 SMB_BSA_CLK
46 SMB_BSA_DATA
88 SMBUS_SMC_BSA_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_BSA_SDA MAKE_BASE=TRUE

DISPLAY TCON
DP RX MASTER FOR MCCS
SMC SLAVE ADDRESS TBD
=SMB_DP_TCON_SCL 78
=SMB_DP_TCON_SDA 78

SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

5 =PP3V3_S0_SMBUS_SMC_MGMT

R5290 1 4.7K 5% 1/16W MF-LF 402 2
R5291 1 4.7K 5% 1/16W MF-LF 402 2

SMC
U4900
(MASTER)

46 SMB_MGMT_CLK
46 SMB_MGMT_DATA
88 SMBUS_SMC_MGMT_SCL MAKE_BASE=TRUE
88 SMBUS_SMC_MGMT_SDA MAKE_BASE=TRUE

DP TX REDRIVER
U9180
(WRITE: 0X9C, READ: 0X9D)
=I2C_DP_DRV_SCL 79
=I2C_DP_DRV_SDA 79

SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE
SMBus Connections

Apple Inc.

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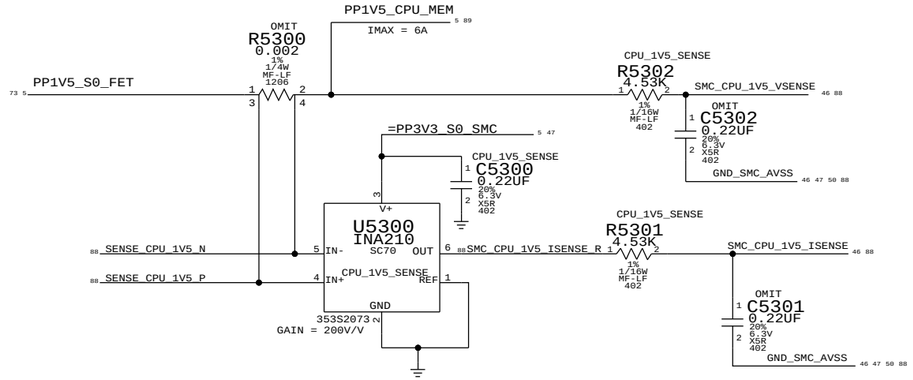
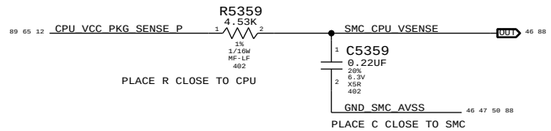
CPU 1.5V CURRENT SENSE



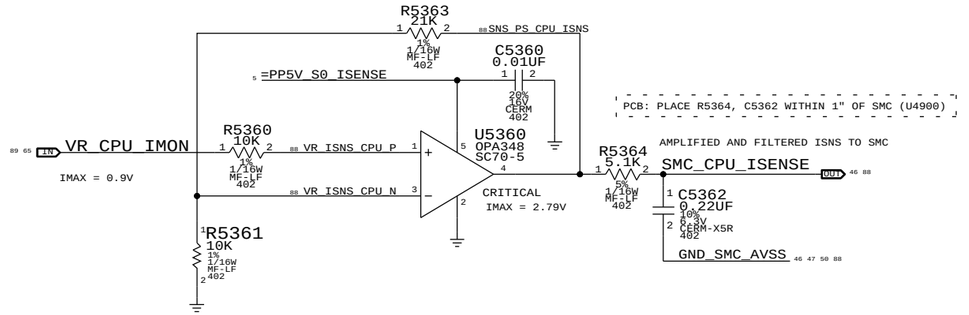
CPU 1.5V VOLTAGE SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	PRODUCTION
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	PRODUCTION

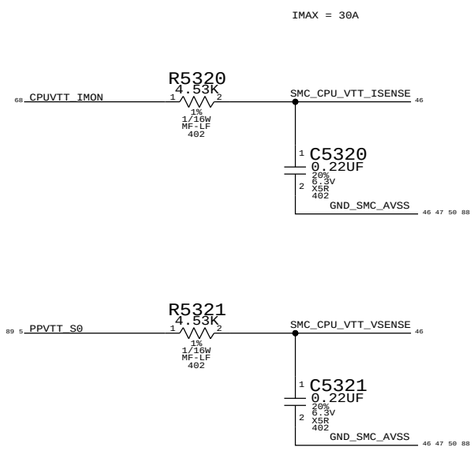
CPU Voltage Sense / Filter



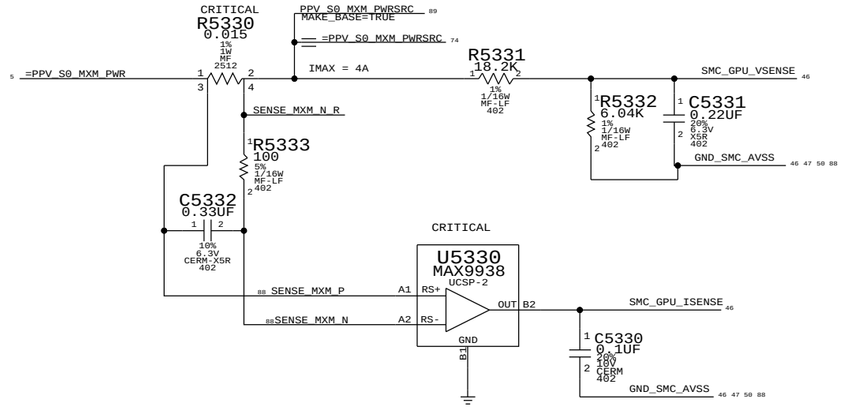
CPU CURRENT SENSE AMP & FILTER



CPU VTT CURRENT SENSE



MXM PWRSRC CURRENT & VOLTAGE SENSE



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU/GPU POWER SENSE

Apple Inc.

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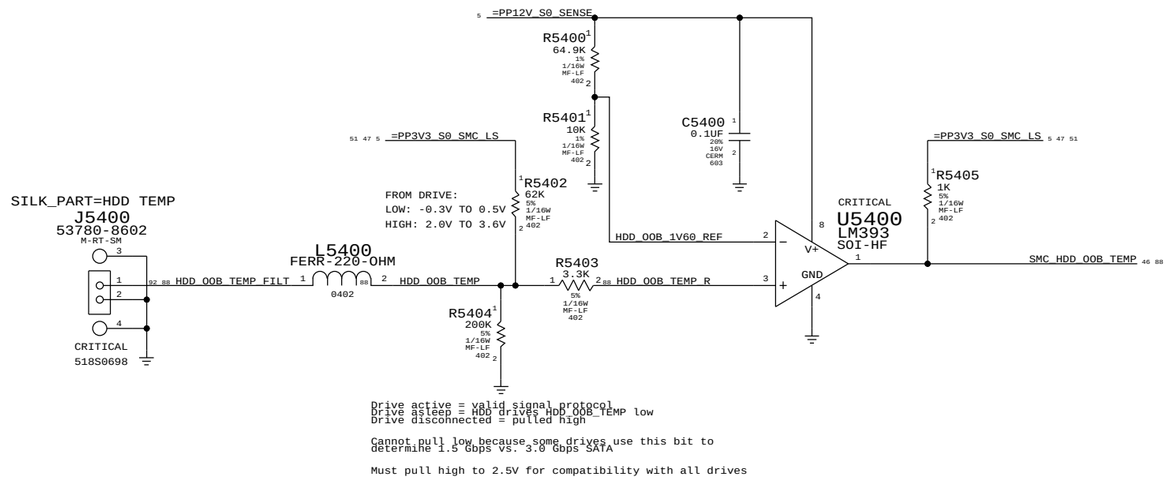
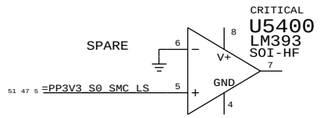
HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



Drive active = valid signal protocol
Drive asleep = HDD drives HDD_OOB_TEMP low
Drive disconnected = pulled high

Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA

Must pull high to 2.5V for compatibility with all drives



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
HDD TEMP SENSE

Apple Inc.

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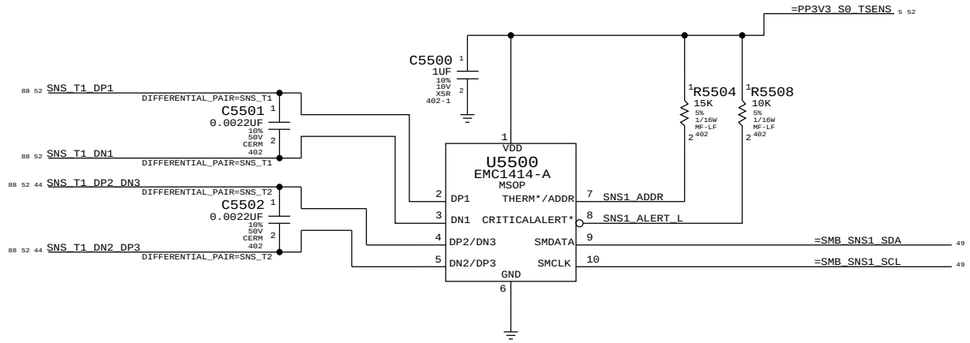
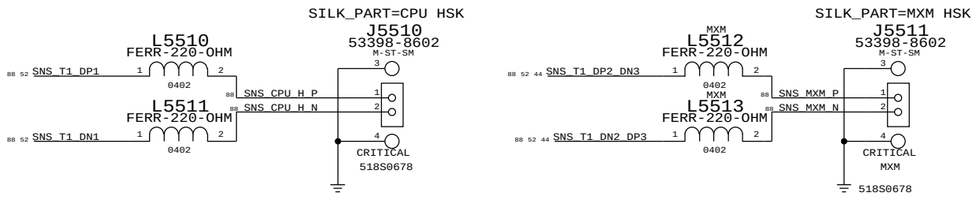
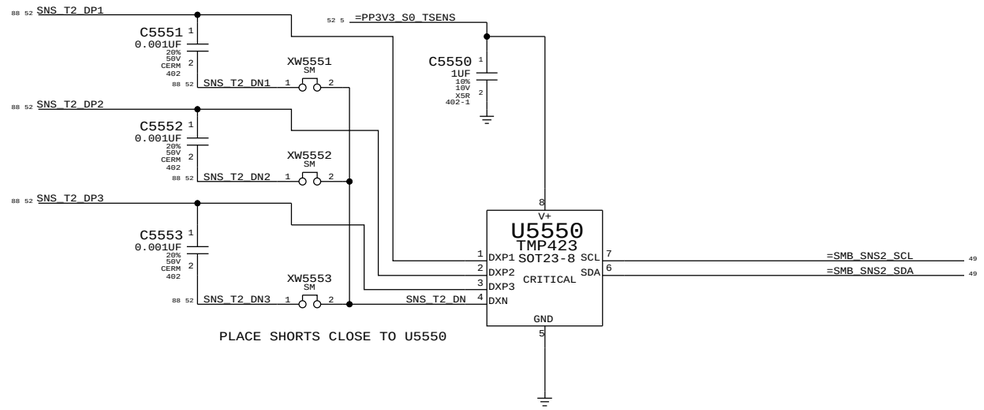
REMOTE HEATSINK SENSORS



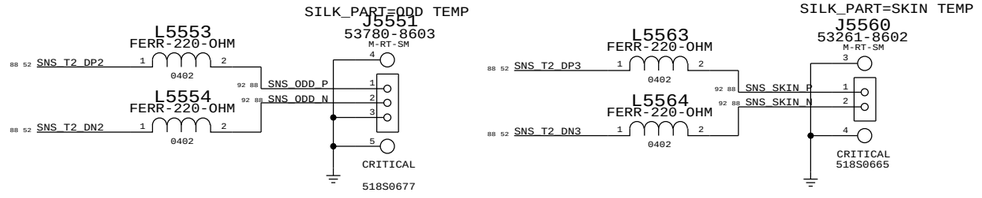
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU



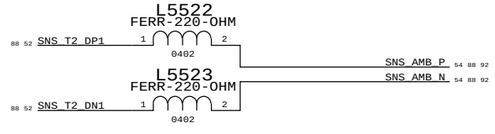
REMOTE SKIN & ODD THERMAL SENSORS



PLACE SHORTS CLOSE TO U5550



AMBIENT SENSE CONNECTOR COMBINED WITH CPU FAN



SYNC_MASTER=NICK SYNC_DATE=11/06/2009

PAGE TITLE: REMOTE TEMP/POWER SENSORS

Apple Inc.

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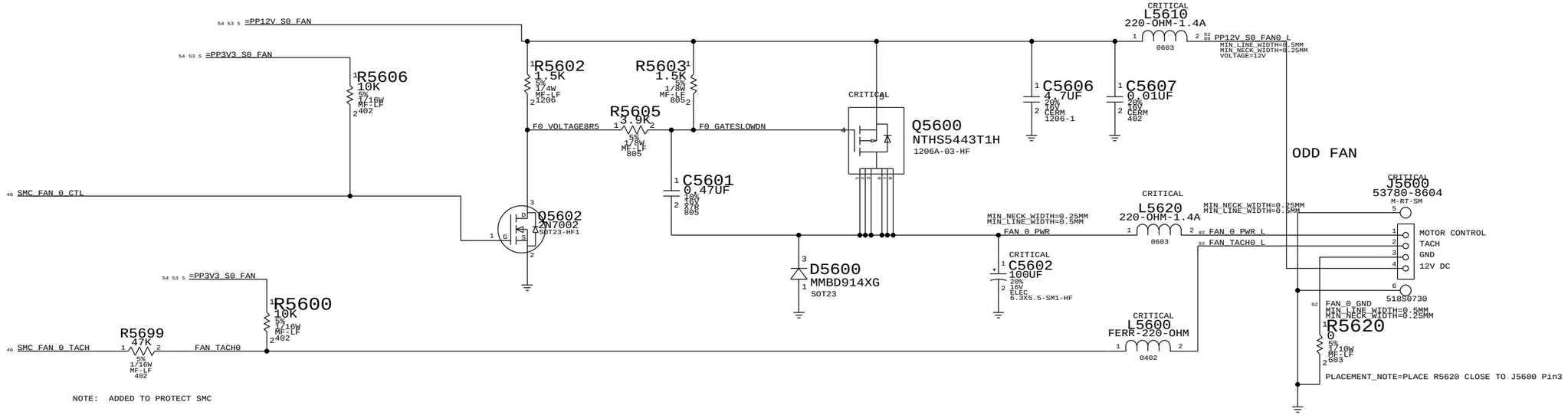
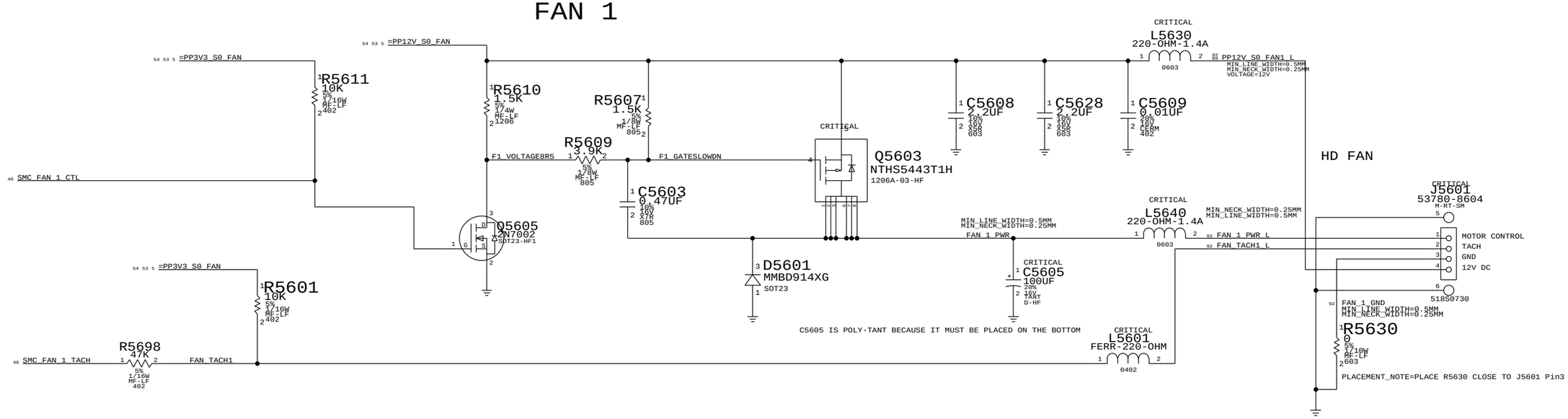
FAN 0



FAN 1



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

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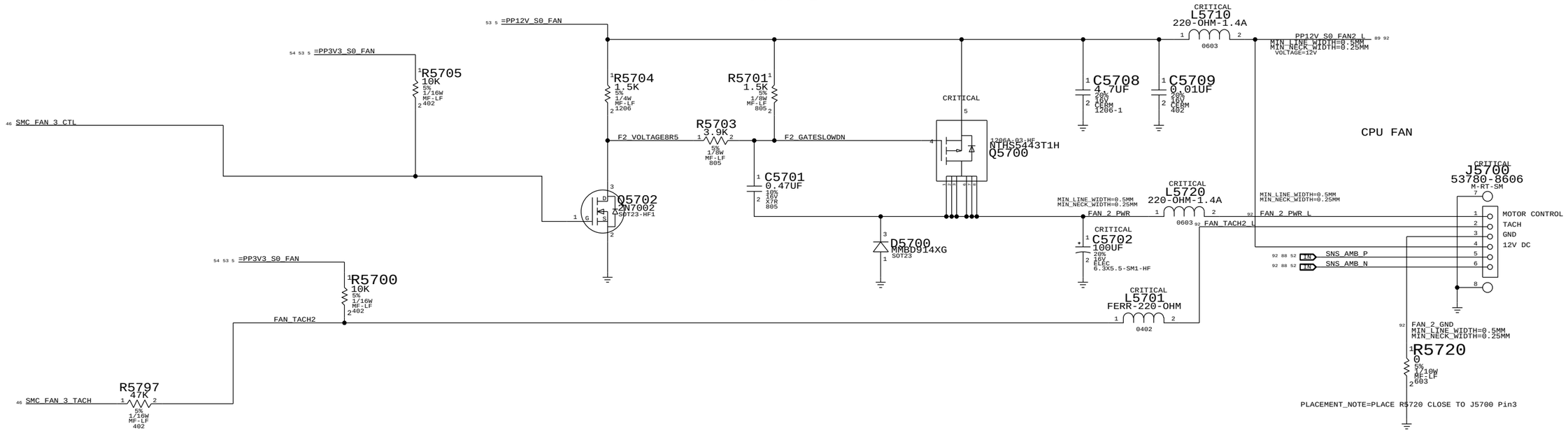
FAN 2 UNUSED

FAN 3



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
CPU FAN & AMBIENT SENSE

Apple Inc.

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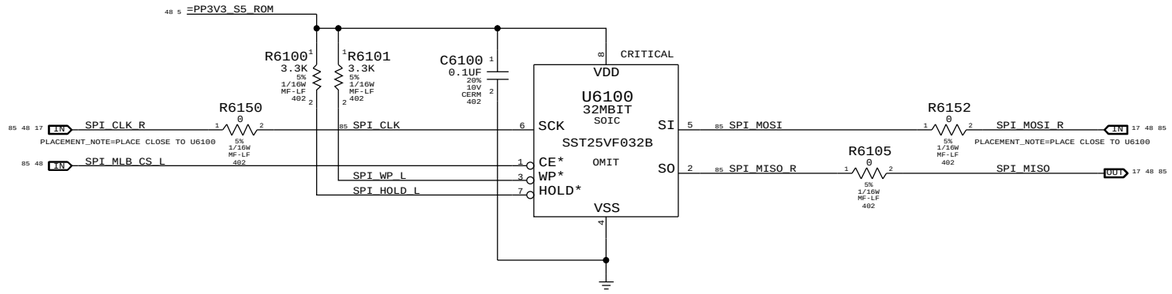

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D

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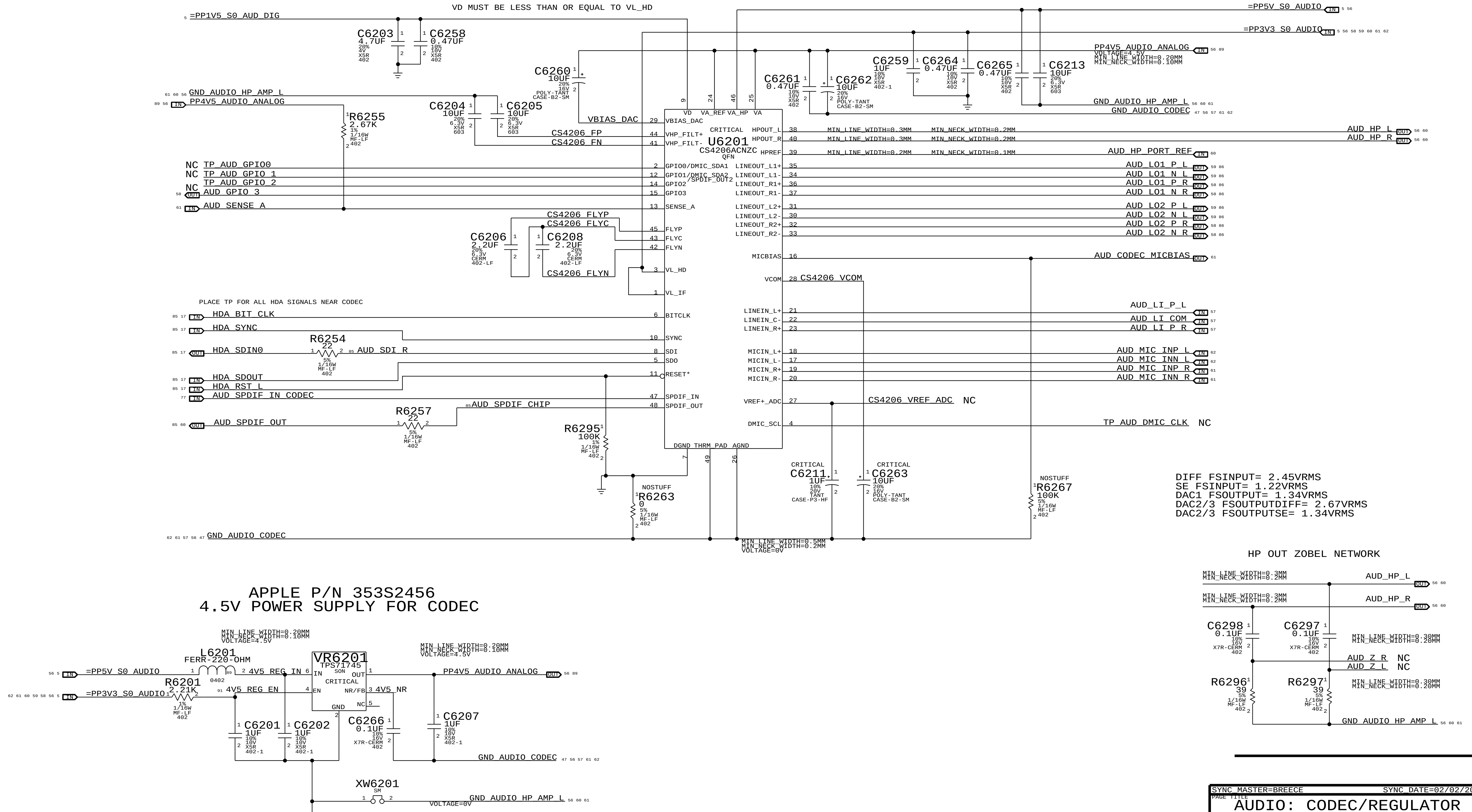
AUDIO CODEC
APPLE P/N 353S2592



SYNC_MASTER=BREECE		SYNC_DATE=02/02/2010
PAGE TITLE: AUDIO: CODEC/REGULATOR		
Apple Inc.	DRAWING NUMBER: 051-8337	SIZE: D
	REVISION: A.0.0	
	BRANCH	
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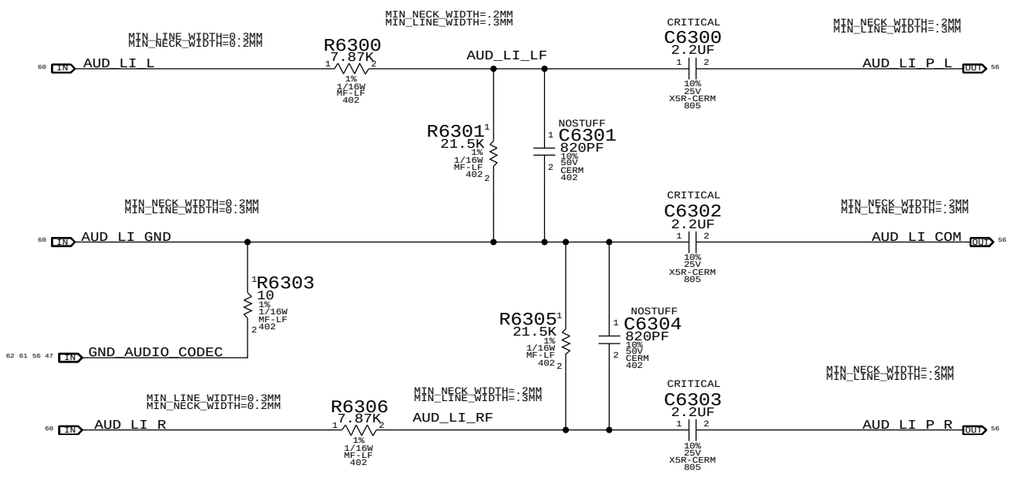
CODEC Nom SE RIN = 20K OHMS
FC = 3.62 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE
AUDIO: FILTER/BUFFER

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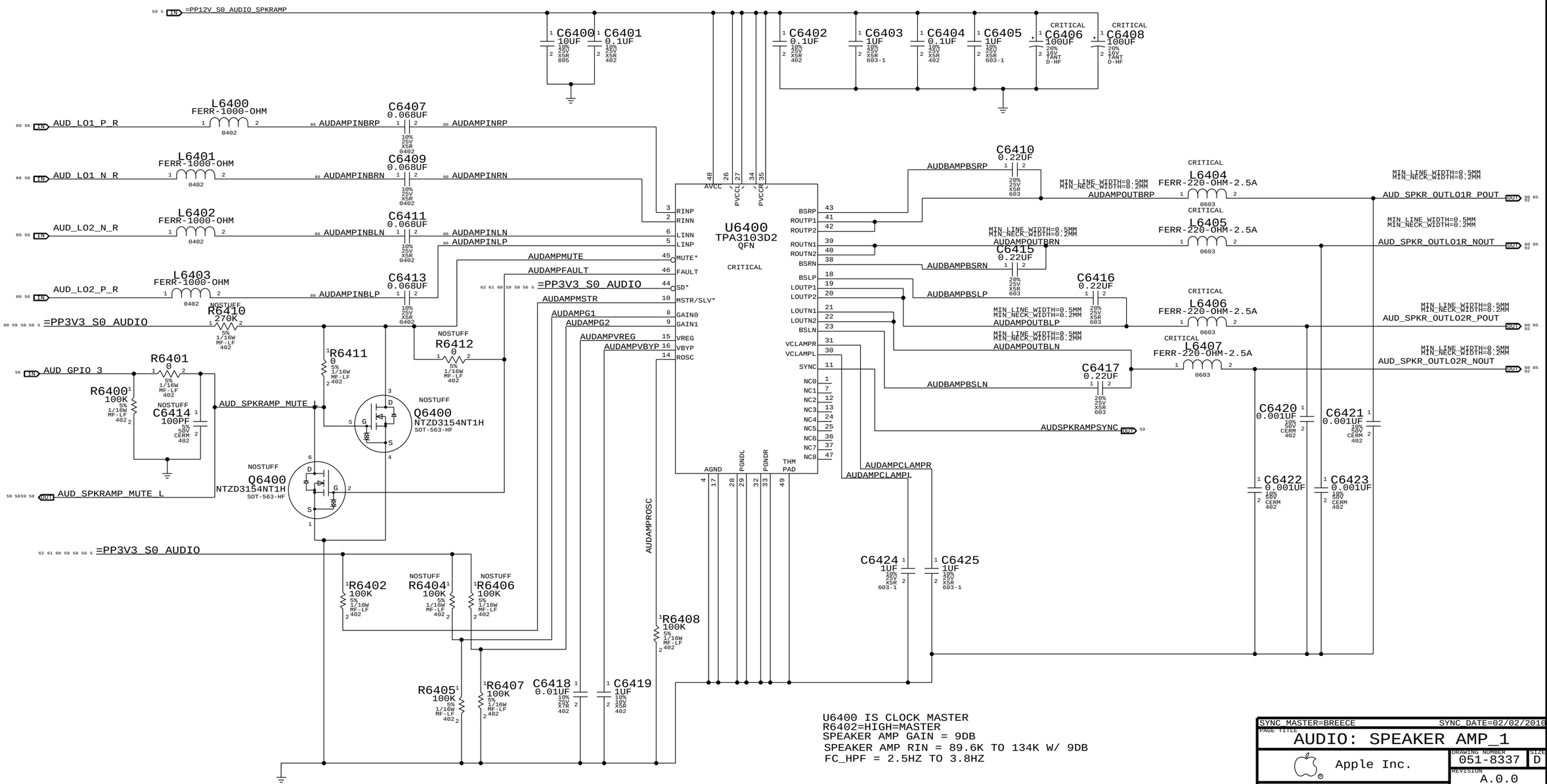
RIGHT CH. SPEAKER AMP
APPLE P/N 353S2768



U6400 IS CLOCK MASTER
R6402=HIGH=MASTER
SPEAKER AMP GAIN = 9DB
SPEAKER AMP RIN = 89.6K TO 134K W/ 9DB
FC_HPF = 2.5HZ TO 3.8HZ

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE
AUDIO: SPEAKER AMP_1

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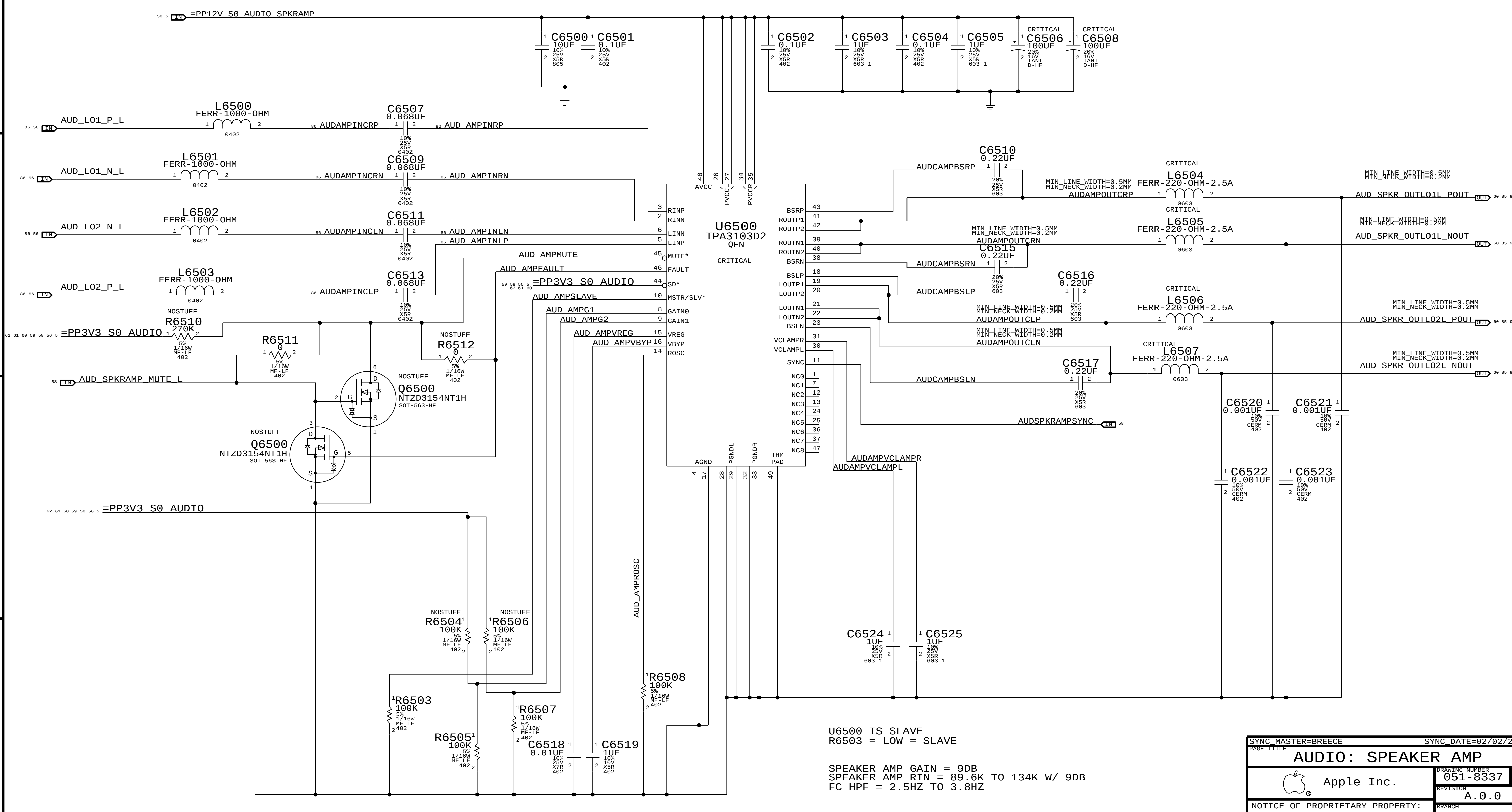
LEFT CH. SPEAKER AMP

APPLE P/N 353S2768


=PP12V_S0_AUDIO_SPKRAMP
C6500 10UF 10% 25V X5R 805
C6501 0.1UF 10% 25V X5R 402
C6502 0.1UF 10% 25V X5R 402
C6503 1UF 10% 25V X5R 603-1
C6504 0.1UF 10% 25V X5R 402
C6505 1UF 10% 25V X5R 603-1
CRITICAL
C6506 100UF 20% 16V TANT D-HF
CRITICAL
C6508 100UF 20% 16V TANT D-HF
AUD_LO1_P_L
L6500 FERR-1000-OHM 0402
AUDAMPINCRP
C6507 0.068UF 10% 25V X5R 0402
AUD_AMPINRP
AUD_LO1_N_L
L6501 FERR-1000-OHM 0402
AUDAMPINCRN
C6509 0.068UF 10% 25V X5R 0402
AUD_AMPINRN
AUD_LO2_N_L
L6502 FERR-1000-OHM 0402
AUDAMPINCLN
C6511 0.068UF 10% 25V X5R 0402
AUD_AMPINLN
AUD_AMPINLP
AUD_LO2_P_L
L6503 FERR-1000-OHM 0402
AUDAMPINCLP
C6513 0.068UF 10% 25V X5R 0402
AUD_AMPMUTE
AUD_AMPFAULT
=PP3V3_S0_AUDIO
AUD_AMPSLAVE
AUD_AMPG1
AUD_AMPG2
AUD_AMPVREG
AUD_AMPVBYP
NOSTUFF
R6510 270K 5% 1/16W MF-LF 402
R6511 0 5% 1/16W MF-LF 402
NOSTUFF
R6512 0 5% 1/16W MF-LF 402
AUD_SPKRAMP_MUTE_L
NOSTUFF
Q6500 NTZD3154NT1H SOT-563-HF
NOSTUFF
Q6500 NTZD3154NT1H SOT-563-HF
U6500 TPA3103D2 QFN
CRITICAL
AVCC PVCCL PVCCR
RINP RINN LINN LINP MUTE* FAULT SD* MSTR/SLV* GAIN0 GAIN1 VREG VBYP ROSC
BSRP ROUTP1 ROUTP2 ROUTN1 ROUTN2 BSRN BSLP LOUTP1 LOUTP2 LOUTN1 LOUTN2 BSLN VCLAMPR VCLAMPL SYNC
NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8
AGND PGNDL PGNDR THM PAD
AUDCAMPBSRP
C6510 0.22UF 20% 25V X5R 603
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDAMPOUTCRP
CRITICAL
L6504 FERR-220-OHM-2.5A 0603
AUD_SPKR_OUTLO1L_POUT
CRITICAL
L6505 FERR-220-OHM-2.5A 0603
AUDAMPOUTCRN
AUD_SPKR_OUTLO1L_NOUT
AUDCAMPBSRN
C6515 0.22UF 20% 25V X5R 603
AUDCAMPBSLP
C6516 0.22UF 20% 25V X5R 603
CRITICAL
L6506 FERR-220-OHM-2.5A 0603
AUDAMPOUTCLP
AUD_SPKR_OUTLO2L_POUT
AUDAMPOUTCLN
CRITICAL
L6507 FERR-220-OHM-2.5A 0603
AUD_SPKR_OUTLO2L_NOUT
AUDCAMPBSLN
C6517 0.22UF 20% 25V X5R 603
AUDSPKRAMPSYNC
AUDAMPVCLAMPR
AUDAMPVCLAMPL
C6520 0.001UF 10% 50V CERM 402
C6521 0.001UF 10% 50V CERM 402
C6522 0.001UF 10% 50V CERM 402
C6523 0.001UF 10% 50V CERM 402
C6524 1UF 10% 25V X5R 603-1
C6525 1UF 10% 25V X5R 603-1
NOSTUFF
R6504 100K 5% 1/16W MF-LF 402
NOSTUFF
R6506 100K 5% 1/16W MF-LF 402
R6503 100K 5% 1/16W MF-LF 402
R6505 100K 5% 1/16W MF-LF 402
R6507 100K 5% 1/16W MF-LF 402
C6518 0.01UF 10% 25V X7R 402
C6519 1UF 10% 10V X5R 402
AUD_AMPROSC
R6508 100K 5% 1/16W MF-LF 402

U6500 IS SLAVE
R6503 = LOW = SLAVE

SPEAKER AMP GAIN = 9DB
SPEAKER AMP RIN = 89.6K TO 134K W/ 9DB
FC_HPF = 2.5HZ TO 3.8HZ

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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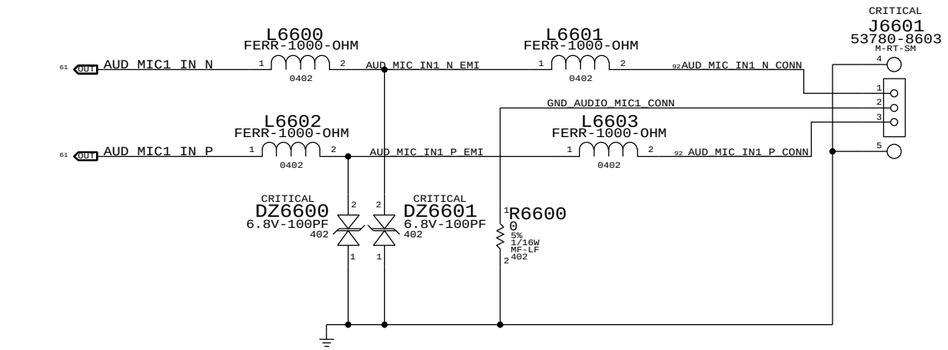
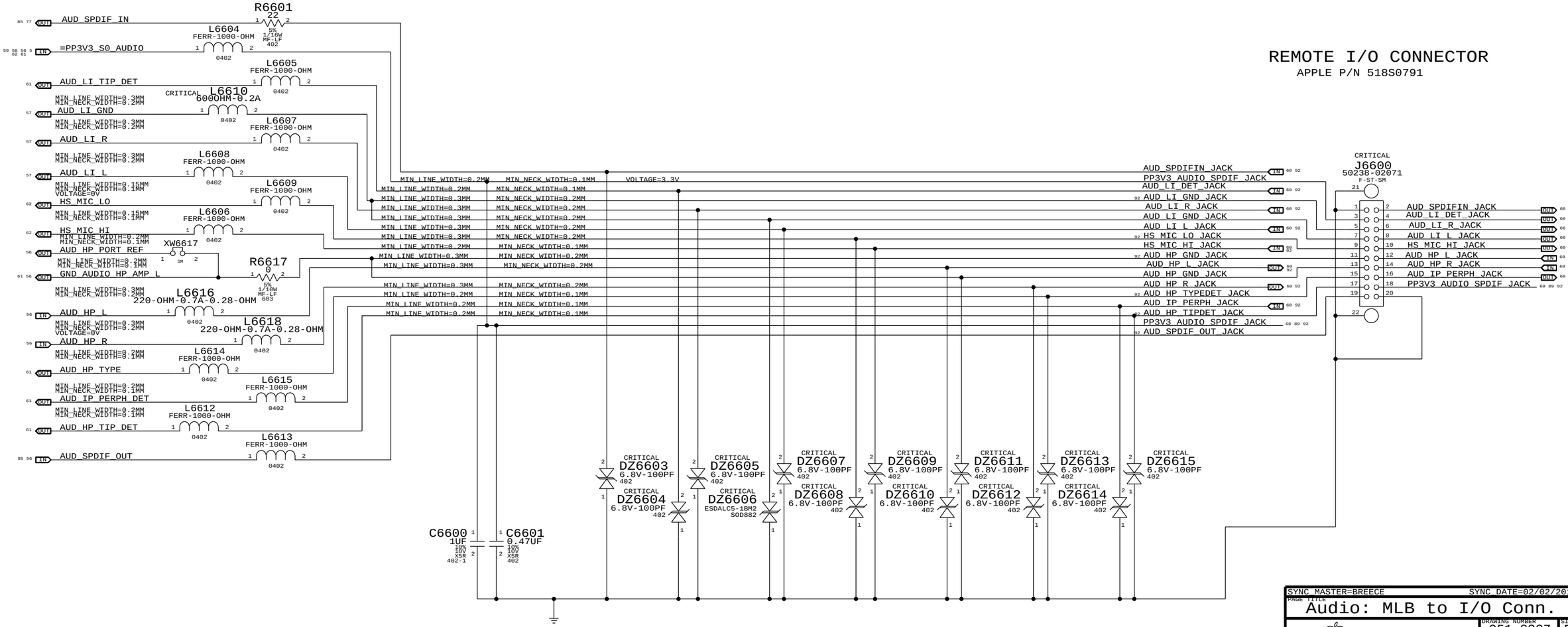
INTERNAL MIC CON
APPLE P/N 518S0677



SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

REMOTE I/O CONNECTOR
APPLE P/N 518S0791



SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

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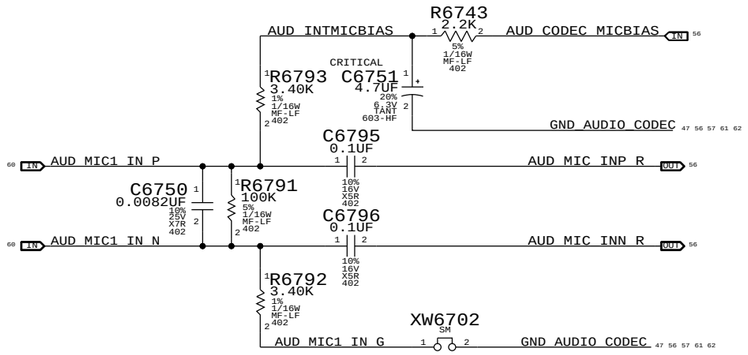
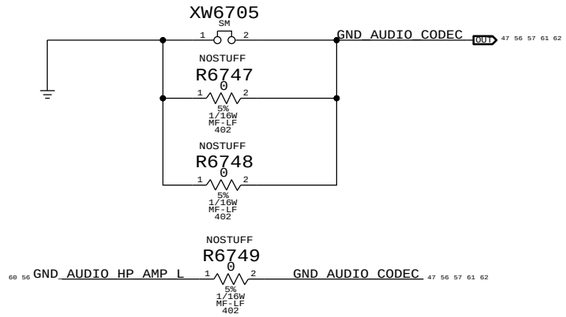
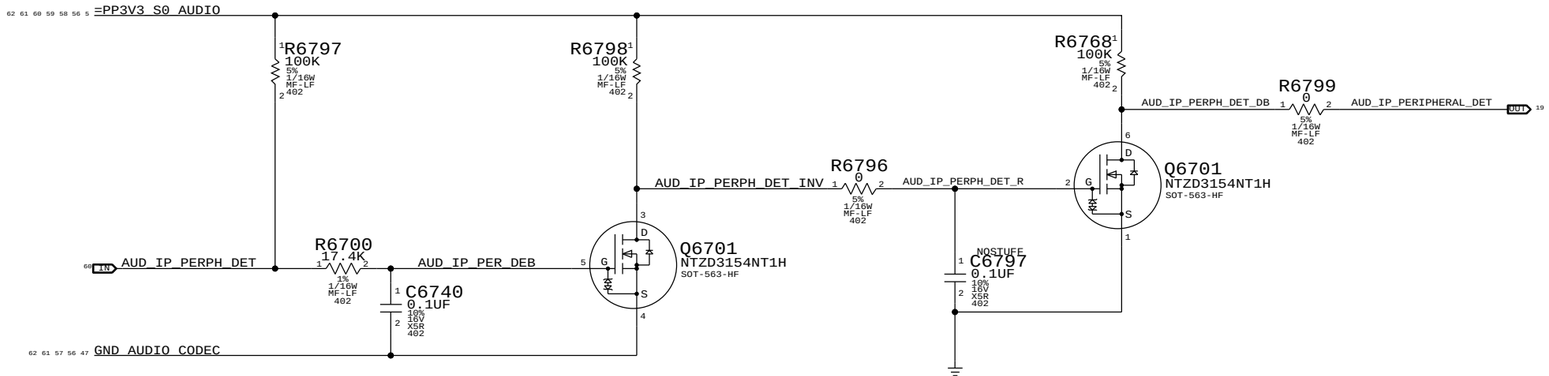
Internal Microphone Impedance Matching



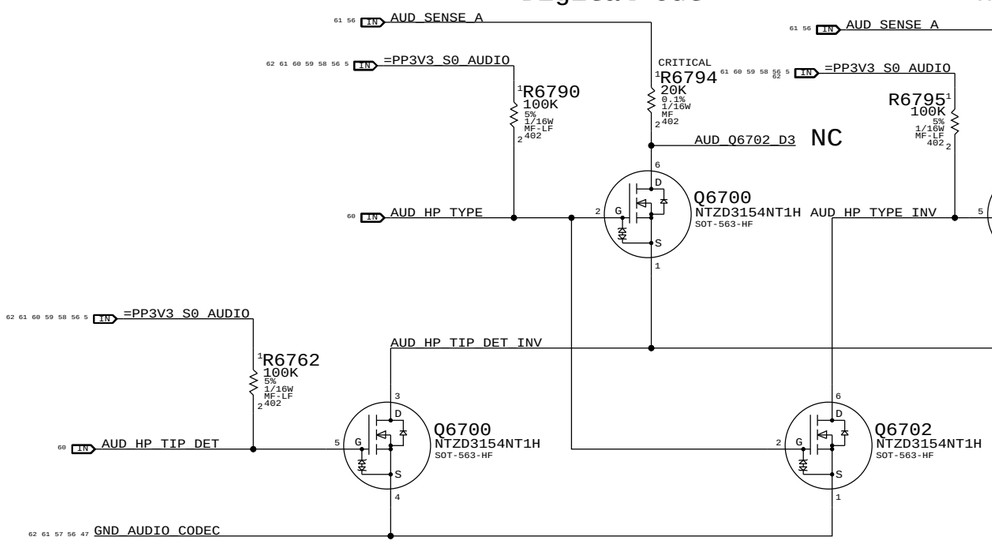
AUDIO STAR GND AND STUFFING OPTIONS



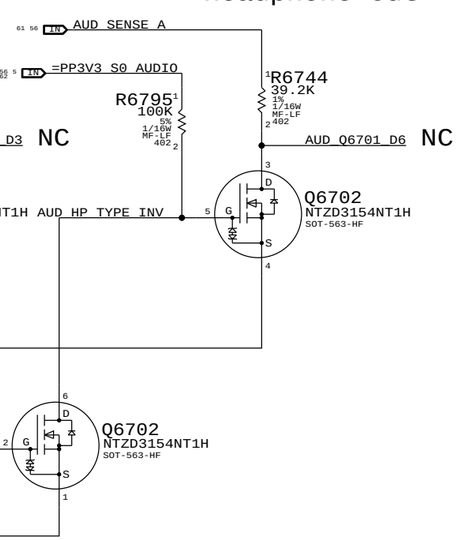
IPHS HS Detect Debounce CKT



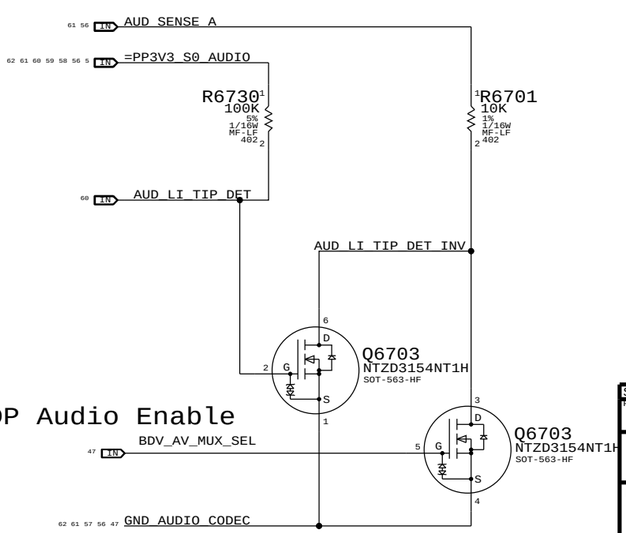
Digital Out



Headphone Out



LI Insert Detect



DP Audio Enable

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE

AUDIO: Detects/Grounding

Apple Inc.

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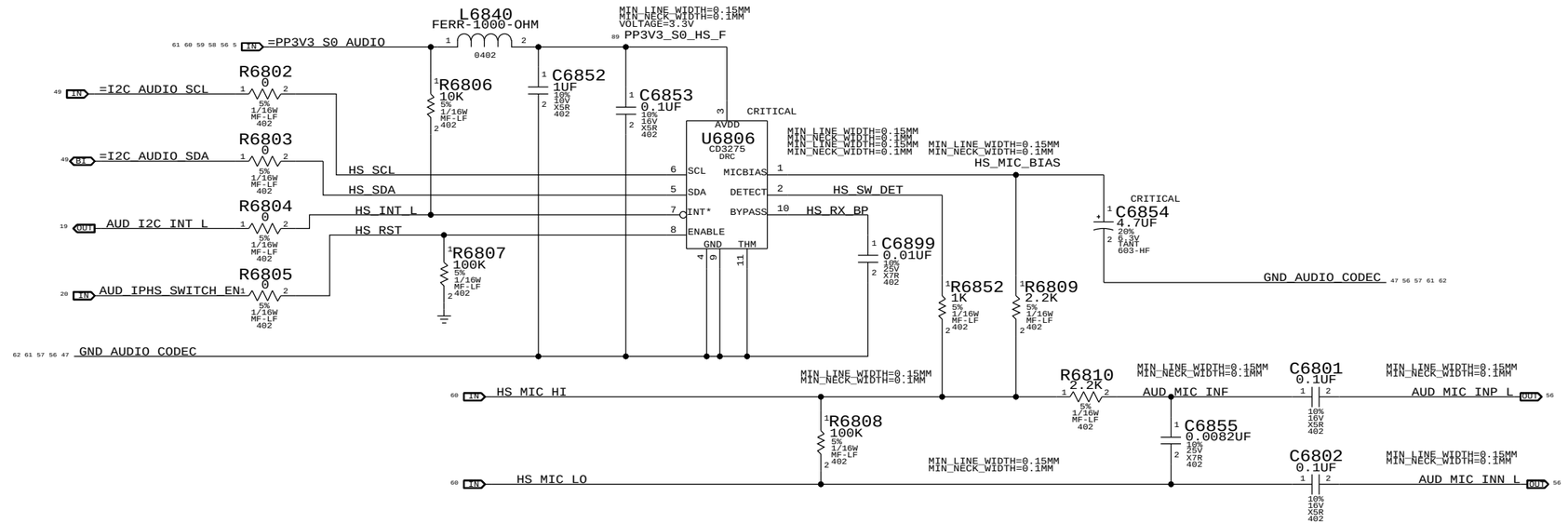
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0D (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256



FLP = 8.82 KHZ
FHP = 80 HZ

SYNC_MASTER=BREECE SYNC_DATE=02/02/2010

PAGE TITLE: AUDIO: Mikey

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State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

R6901 0 5% 1/16W MF-LF 402
91 48 IN PM_RSMRST_L 1 2 PM_RSMRST_PCH_L OUT 18 91

SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

73 64 63 5 =PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 50V CERM 402
DDRVTT_EN 63 71 91
NOSTUFF C6953 0.1UF 10% 16V X5R 402
VTT_REG_PGOOD_L 5
Q6911 MMDT3904-X-G SOT-363-LF
91 68 64 63 10 CPUVTT_REG_PGOOD
R6950 100K 5% 1/16W MF-LF 402
CPUVTT_REG_PGOOD_R
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

64 63 10 5 =PP3V3_S5_PWRCTL
C6910 0.1UF 20% 10V CERM 402
91 18 PM_SLP_S4_1_L
U6900 74LVC08 TSSOP-HF 08
S4_ENABLES
R6911 33 5% 1/16W MF-LF 402
R6912 33 5% 1/16W MF-LF 402
P3V3S3_EN 73 91
Enable FET
P5VS3_EN 70 91
ENABLE REGULATOR
NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

64 63 10 5 =PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
18 CPU_SKTOCC_L
Q6910 2N7002 SOT23-HF
NOSTUFF R6917 0 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

5 =PP5V_S3_PWRCTL
R6910 100K 5% 1/16W MF-LF 402
70 P5VS3_REG_PGOOD
MAKE_BASE=TRUE
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402
PM_EN_USB_PWR 43
=DDRREG_EN 71

SLP_S3 ENABLES

UNUSED
64 63 10 5 =PP3V3_S5_PWRCTL
U6900 74LVC08 TSSOP-HF 08

ME RAILS TIED TO S0 ONLY
91 18 PM_SLP_M_L
TP_PM_SLP_M_L
MAKE_BASE=TRUE

64 63 10 5 =PP3V3_S5_PWRCTL
91 81 64 47 46 36 26 18 5 PM_SLP_S3_L
U6900 74LVC08 TSSOP-HF 08
(PM_SLP_S3_L_BUF)
PM_SLP_S3_BUF_L
MAKE_BASE=TRUE
R6946 33 5% 1/16W MF-LF 402
R6947 33 5% 1/16W MF-LF 402
P3V3S0_EN
Enable FET
P5VS0_EN
Enable FET
OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)
R6944 10K 1% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
64 PGOOD_P12V_S0
MAKE_BASE=TRUE
PM_SLP_S3_BUF_L 63 63
91 71 PM_PGOOD_DDRREG_S3
Enable FET
P1V5_S0_EN 73 91
DDRVTT_EN 63 71 91
Enable regulator
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

73 64 63 5 =PP3V3_S0_PWRCTL
R6942 10K 5% 1/16W MF-LF 402
91 73 PGOOD_P5V_S0
MAKE_BASE=TRUE
C6942 1UF 10% 6.3V CERM 402
Enable regulator
PCHCORE_REG_EN
PCHCORE VREG
69 91 91 69 64
PCHCORE_REG_PGOOD
MAKE_BASE=TRUE
ENABLE FET
P1V05_ME_S0_EN
Enable regulator
CPUVTT_REG_EN
CPUVTT VREG
68 91 91 68 64 63 10
CPUVTT_REG_PGOOD
MAKE_BASE=TRUE
Enable regulator
PM_EN_PVCORE_CPU 65
TO ENABLE OF CPU VREG

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A
PAGE TITLE
POWER SEQUENCING ENABLES

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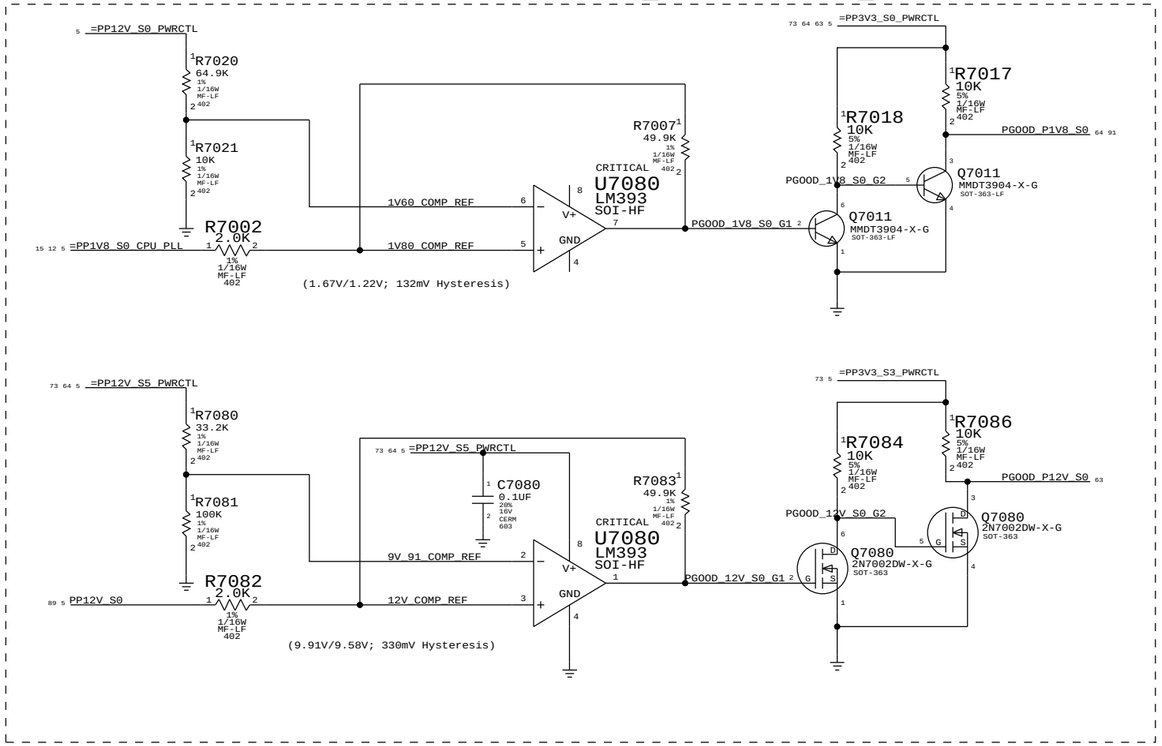
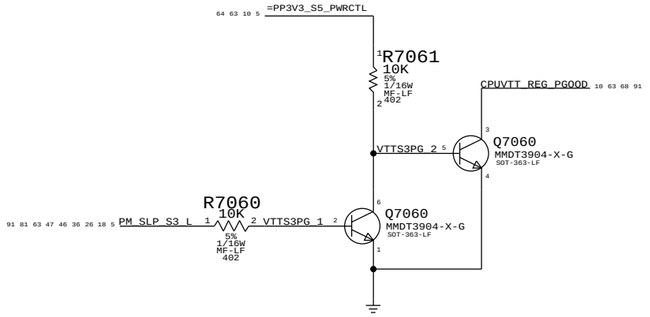
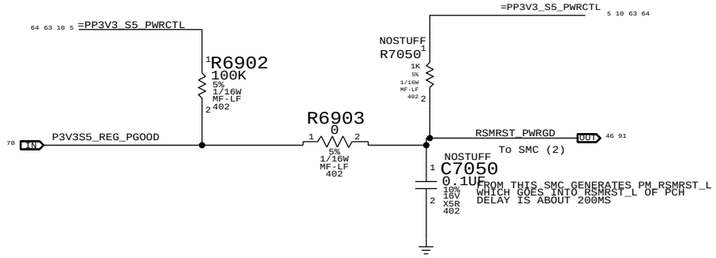
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

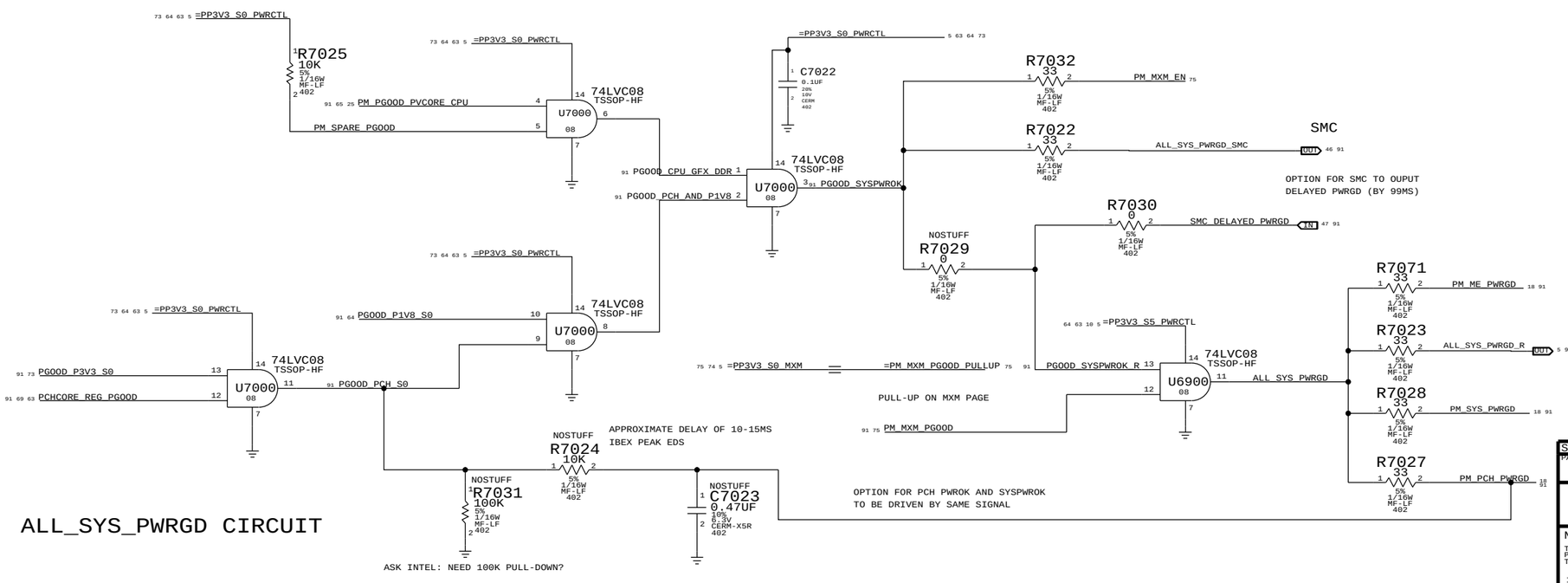


S0 RAILS PGOOD



DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)





ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: POWER SEQUENCING PGOOD

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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CPU CORE REG 1.1V/???A O/P= PPVCORE_S0_CPU_REG

CPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

=PP5V_S0_VRD
PPVCORE_S0_CPU_REG
CPU_VCC_PKG_SENSE_P
CPU_VCC_PKG_SENSE_N
PP5V_S0_CPU_VCORE_VCC
=PP3V3_S0_VRD
=PPVTT_S0_CPU
PM_EN_PVCORE_CPU
PM_PGOOD_PVCORE_CPU
VR_CPU_IOUT
CPU_PSI_L
CPU_VID<7..0>
=PP12V_S0_VRD
IMAX = 10.5A
PP12V_S0_CPU_FLTRD
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE

R7118 2.2 1% 1/10W MF-LF 805
PP5V_S0_CPU_VCORE_VCC
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V

XW7120 OMIT SM
R7127 1K 1% 1/10W MF-LF 402
R7139 10 1% 1/10W MF-LF 402
R7128 0 5% 1/16W MF-LF 402
VR_CPU_VSNS_XW_P
VOLTAGE=1.1V
NET_PHYSICAL_TYPE=SNS_DIFF
VR_CPU_VSNS_R_P
VR_CPU_VSEN
SIGNAL_MODEL=EMPTY
1.25 mOhm loadline
NOSTUFF C7101 0.0022UF 10% 50V CERM 402
R7129 0 5% 1/16W MF-LF 402
VR_CPU_VSNS_R_N
R7137 10 1% 1/10W MF-LF 402
VR_CPU_RGND
XW7130 SM
VR_CPU_VSNS_XW_N
VOLTAGE=0V
NET_PHYSICAL_TYPE=SNS_DIFF
R7138 1K 1% 1/10W MF-LF 402
C7102 0.0022UF 10% 50V CERM 402
C7103 0.0022UF 10% 50V CERM 402
AGND_CPU

C7104 47PF 5% 50V CERM 402
VR_CPU_FB_R
VR_CPU_COMP_R
R7101 16.5K 1% 1/16W MF-LF 402
VR_CPU_COMP_RC
C7105 0.0022UF 10% 50V CERM 402
R7179 0 5% 1/16W MF-LF 402
LOCAL 5V
R7102 1K 1% 1/16W MF-LF 402
VR_VDF_R1
R7103 287 1% 1/16W MF-LF 402
NOSTUFF R7146 1M 5% 1/16W MF-LF 402
R7104 0 5% 1/16W MF-LF 402
C7107 1UF 10% 16V X5R 402
AGND_CPU
C7106 470PF 10% 50V CERM 402
VR_VDF_R2
R7149 47.5 1% 1/10W MF-LF 402
VR_CPU_COMP
VR_CPU_FB

NOSTUFF R7147 0 5% 1/16W MF-LF 402
NOSTUFF R7148 0 5% 1/16W MF-LF 402
R7144 0 5% 1/16W MF-LF 402
VR_CPU_PWM1
R7131 165 1% 1/10W MF-LF 402
VR_CPU_ISNS1_RR_2
R7132 0 5% 1/10W MF-LF 402
NOSTUFF C7130 15PF 1% 50V C0G 402
C7131 150PF 5% 50V CERM 402
C7132 0.1UF 10% 16V X5R 402
C7133 220PF 5% 25V CERM 402
DIFFERENTIAL_PAIR=VR_CPU_ISNS1
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N
R7133 1.02K 1% 1/10W MF-LF 402

CRITICAL
SYM_VER_2
U7100
QFN
ISL6334
VCC 19
PWM1 26
ISEN1+ 28
ISEN1- 27
VR_CPU_ISNS1_R_P
VR_CPU_ISNS1_R_N
PWM2 20
ISEN2+ 22
ISEN2- 21
VR_CPU_PWM2_R
VR_CPU_ISNS2_R_P
VR_CPU_ISNS2_R_N
PWM3 31
ISEN3+ 29
ISEN3- 30
VR_CPU_PWM3_R
PWM4 25
ISEN4+ 23
ISEN4- 24
VR_CPU_PWM4_R
CRITICAL
VSS 41
THRM_PAD
EN_PWR 32

R7140 0 5% 1/16W MF-LF 402
VR_CPU_PWM2
R7141 165 1% 1/10W MF-LF 402
VR_CPU_ISNS2_RR_2
R7142 0 5% 1/10W MF-LF 402
NOSTUFF C7140 15PF 1% 50V C0G 402
C7141 150PF 5% 50V CERM 402
C7142 0.1UF 10% 16V X5R 402
C7143 220PF 5% 25V CERM 402
DIFFERENTIAL_PAIR=VR_CPU_ISNS2
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N
R7143 1.02K 1% 1/10W MF-LF 402

R7150 0 5% 1/16W MF-LF 402
VR_CPU_PWM3
R7151 165 1% 1/10W MF-LF 402
VR_CPU_ISNS3_RR_2
R7152 0 5% 1/10W MF-LF 402
NOSTUFF C7150 15PF 1% 50V C0G 402
C7151 150PF 5% 50V CERM 402
C7152 0.1UF 10% 16V X5R 402
C7153 220PF 5% 25V CERM 402
DIFFERENTIAL_PAIR=VR_CPU_ISNS3
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N
R7153 1.02K 1% 1/10W MF-LF 402
AGND_CPU

VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.
LAYOUT: PLACE RT7101 NEAR HOT SPOT
R7100 1.02K 1% 1/10W MF-LF 402
NOSTUFF R7105 20.0K 1% 1/10W MF-LF 402
NOSTUFF R7178 0 5% 1/10W MF-LF 402
NOSTUFF R7177 0 5% 1/10W MF-LF 402
RT7101 6.8K 0603
C7180 0.1UF 20% 10V CERM 402
R7106 0 5% 1/10W MF-LF 402
R7107 21K 1% 1/10W MF-LF 402
R7108 75K 1% 1/10W MF-LF 402
R7109 100K 1% 1/10W MF-LF 402
C7110 1500PF 10% 25V X7R 402
R7110 1K 1% 1/10W MF-LF 402
VR_CPU_TCOMP
VR_CPU_OFS
VR_CPU_FS
VR_CPU_SS
VR_CPU_DAC
VR_CPU_REF
VR_CPU_TM
VR_CPU_EN_VTT
VR_CPU_VDIFF
VR_CPU_PSI_L
VR_CPU_IMON
VR_CPU_FAN
VR_CPU_VRDHOT
VR_CPU_EN_PWR

R7111 0 5% 1/16W MF-LF 402
NOSTUFF C7109 0.01UF 10% 16V CERM 402
R7112 2.0K 1% 1/10W MF-LF 402
NOSTUFF R7172 1.02K 1% 1/16W MF-LF 402
R7114 49.9K 1% 1/16W MF-LF 402
R7115 49.9K 1% 1/16W MF-LF 402
R7145 0 5% 1/16W MF-LF 402
NOSTUFF D7171 NSR0140P2T5G SOD-923-HF
R7171 0 5% 1/16W MF-LF 402
NOSTUFF C7171 0.020UF 10% 50V CERM 402
R7117 10K 1% 1/10W MF-LF 402
C7112 0.022UF 10% 16V CERM-X5R 402
R7116 1.54K 1% 1/10W MF-LF 402
VR_CPU_IOUT_PD
OMIT XW7101 SM
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0V
R7136 10K 5% 1/16W MF-LF 402
R7135 1K 5% 1/16W MF-LF 402
C7135 0.001UF 10% 50V CERM 402

CRITICAL
L7100
1UH-20A-4.5MOHM
TH-VERT-HF
152-0110

CPU CORE INPUT Filtering

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A
PAGE TITLE
VREG: PPVCORE_S0_CPU
Apple Inc.
DRAWING NUMBER 051-8337
SIZE D
REVISION A.0.0
BRANCH
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SHEET 65 OF 92

SYNC_MASTER=K74_MASTER	SYNC_DATE=N/A
PAGE TITLE: VREG: CPU CORE - PHASES 1-3	
Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
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	PAGE: 72 OF 110
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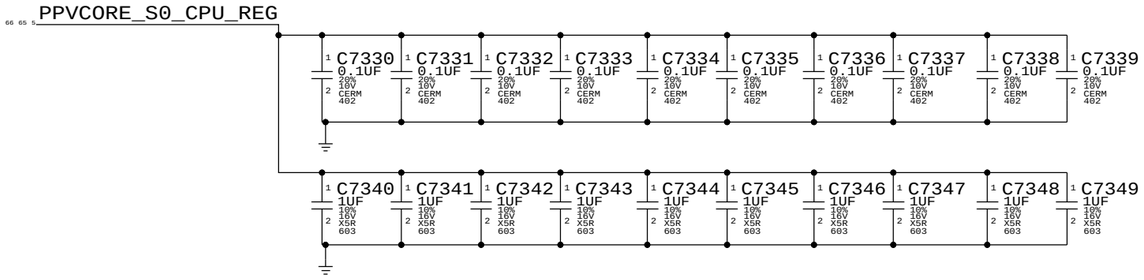

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
VREG: CPU CORE - CAPS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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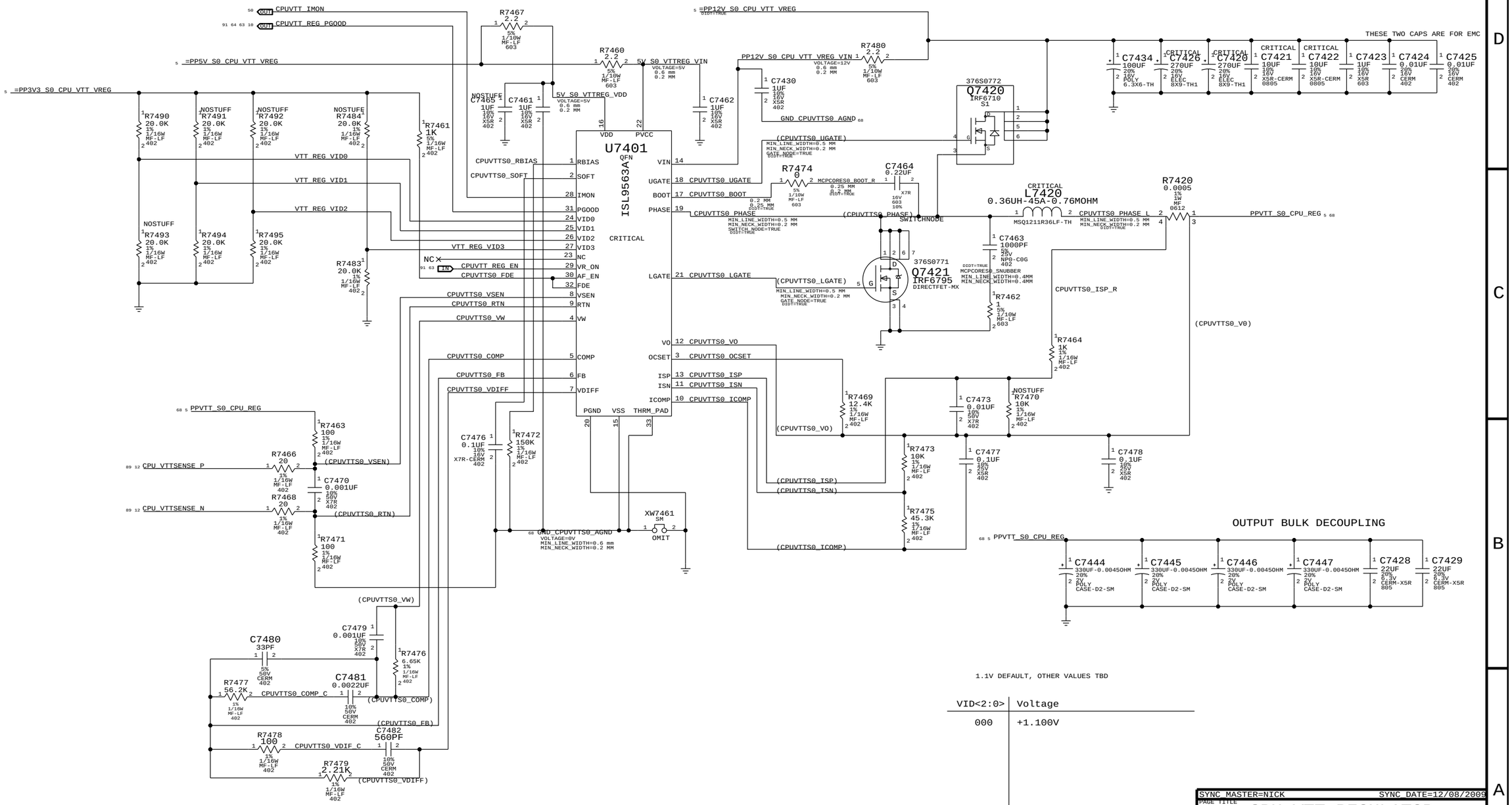
CPU VTT REG 1.1V O/P= PPVTT_S0_CPU_REG



1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE: CPU VTT REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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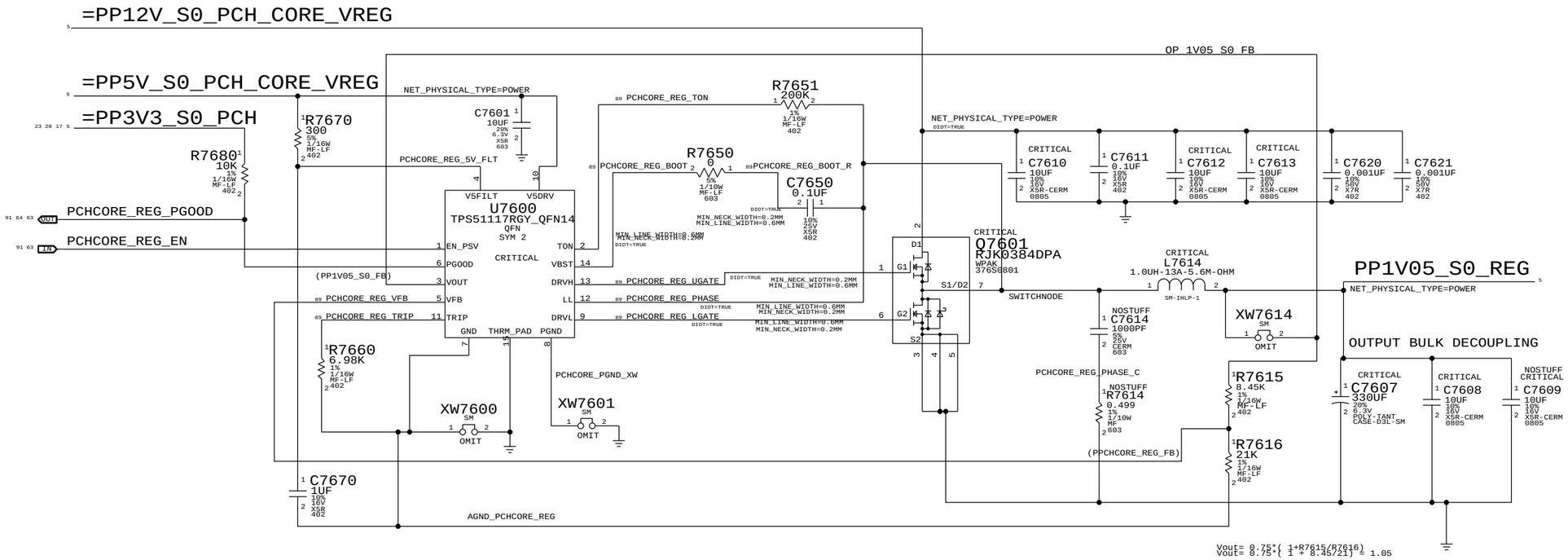
IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: IBEX PEAK CORE

Apple Inc.

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3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

=PP12V_S5_P5VS3_VREG

=PP12V_S5_P3V3S5_VREG

NET_PHYSICAL_TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6.3X6-TH
C7719 100UF 20% 16V POLY 6.3X6-TH
C7712 10UF 10% 16V X5R-CERM 0805
C7710 10UF 10% 16V X5R-CERM 0805
C7711 0.1UF 10% 16V X5R 402
C7722 0.1UF 10% 16V X5R 402

C7766 270UF 20% 16V ELEC 8X9-TH1
C7783 22UF 20% 16V X7R 1210
C7751 10UF 10% 16V X5R-CERM 0805
C7752 10UF 10% 16V X5R-CERM 0805
C7753 10UF 10% 16V X5R-CERM 0805
C7758 10UF 10% 16V X5R-CERM 0805
C7765 10UF 10% 16V X5R-CERM 0805

PP5V_S5_LDO

EMC: C7754,C7755
PLACE AT Q7330

C7754 0.1UF 10% 25V X5R 402
C7755 0.1UF 10% 25V X5R 402

DIDT=TRUE

3V3 OUTPUT

PP3V3_S5_REG

CRITICAL
L7710 2.2UH-14A
MMD06CZ-SM

SWITCHNODE

NET_PHYSICAL_TYPE=POWER

Q7710
RJK0384DPA
WPAK
376S0801

D1
G1
S1/D2
G2
S2

1 (P3V3S5_UGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE

6 (P3V3S5_LGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE

C7790 8200PF 10% 50V CERM 603
R7790 16.5K 1% 1/16W MF-LF 402
R7791 16.5K 1% 1/16W MF-LF 402

C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF
R7730 0.499 1% 1/10W MF 603 NOSTUFF

P3V3S5_REG_SNUB

C7714 0.1UF 10% 50V X7R 603-1

R7710 0 5% 1/10W MF-LF 603

P3V3S5_REG_BOOT_R

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM

(P3V3S5_PHASE)

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM

U7700
ISL62383
QFN
CRITICAL

P3V3S5_REG_PGOOD	7	PGOOD1	PGOOD2	1
P3V3S5_REG_UGATE	14	UGATE1	UGATE2	22 P5VS3_REG_UGATE
P3V3S5_REG_BOOT	15	BOOT1	BOOT2	21 P5VS3_REG_BOOT
P3V3S5_REG_PHASE	13	PHASE1	PHASE2	23 P5VS3_REG_PHASE
P3V3S5_REG_LGATE	16	LGATE1	LGATE2	20 P5VS3_REG_LGATE
P3V3S5_REG_ISEN	10	ISEN1	ISEN2	26 P5VS3_REG_ISEN
P3V3S5_REG_OCSET	11	OCSET1	OCSET2	25 P5VS3_REG_OCSET
P3V3S5_REG_VOUT1	9	VOUT1	VOUT2	27 P5VS3_REG_VOUT2
P3V3S5_REG_FB	8	FB1	FB2	28 P5VS3_REG_FB
	6	FSET1	FSET2	2 P5VS3_REG_FSET2
	12	EN1	EN2	24
	18	LDO5	VIN	17
		FCCM		3 TP_P5VS3_REG_FCCM
		THRM PAD	PGND	

P3V3S5_12VE_EN1

C7742 4.7UF 20% 6.3V CERM 603
R7740 2.2 5% 1/8W MF-LF 805
P5V_S5_LDO_R
P5V_S5_VCC1
C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603

P5VS3_REG_PGOOD

Q7750
CSD58851Q5A
MLP5X6-LFPAK-Q5A
376S0631
CRITICAL

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2 MM

P5VS3_REG_BOOT_R

R7750 0 5% 1/10W MF-LF 603
C7756 0.1UF 10% 25V X5R 402

MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6MM

NOSTUFF
C7757 0.001UF 10% 50V CERM 402

5V_SNUBBER

R7752 0.499 1% 1/10W MF 603 NOSTUFF

Q7751
CSD58851Q5A
MLP5X6-LFPAK-Q5A
376S0631
CRITICAL

D7750
CTLSH3-30M833
TLM833
CRITICAL

R7770 14.3K 1% 1/10W MF-LF 402
C7770 0.01UF 10% 16V CERM 402

R7771 14.3K 1% 1/16W MF-LF 402

5V OUTPUT

EMC: C7763,C7764
PLACE AT L7750.2

C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

CRITICAL
L7750
2.2UH-10A-12.5MOHM
PAB0705AR-SM

PP5V_S3_REG

NET_PHYSICAL_TYPE=POWER

OUTPUT BULK DECOUPLING:

C7760 10UF 20% 6.3V CERM 805-1
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL
CRITICAL

SM XW7751 OMIT

OUTPUT BULK DECOUPLING:

PLACEMENT_NOTE=PLACE NEXT TO C7716

C7715 10UF 10% 16V X5R-CERM 0805
C7717 10UF 10% 16V X5R-CERM 0805
128S0237
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL

SM XW7716 OMIT

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>
R7721 10.0K 0.5% 1/16W MF 402 <Rb>
R7724 976 1% 1/10W MF-LF 402
P3V3S5_REG_FB_R
C7720 1000PF 5% 25V NP0-C0G 402

C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603

EMC CAPS
PLACE CLOSE
TO L

Vout = 0.6V * (1 + Ra / Rb)

R7722 68K 5% 1/16W MF-LF 402
R7723 33K 5% 1/16W MF-LF 402

P3V3S5_REG_FSET1
C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402

P5VS3_REG_FB_R
R7759 976 1% 1/16W MF-LF 402
C7759 1000PF 5% 25V NP0-C0G 402
R7755 75K 1% 1/16W MF-LF 402 RA
R7756 10K 1% 1/16W MF-LF 402 RB

C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402

NOSTUFF
C7777 0.001UF 10% 50V CERM 402

P5VS3_EN

SYNC_MASTER=NICK SYNC_DATE=12/08/2009

PAGE TITLE
5V_S3 / 3V3_S5 VREGS

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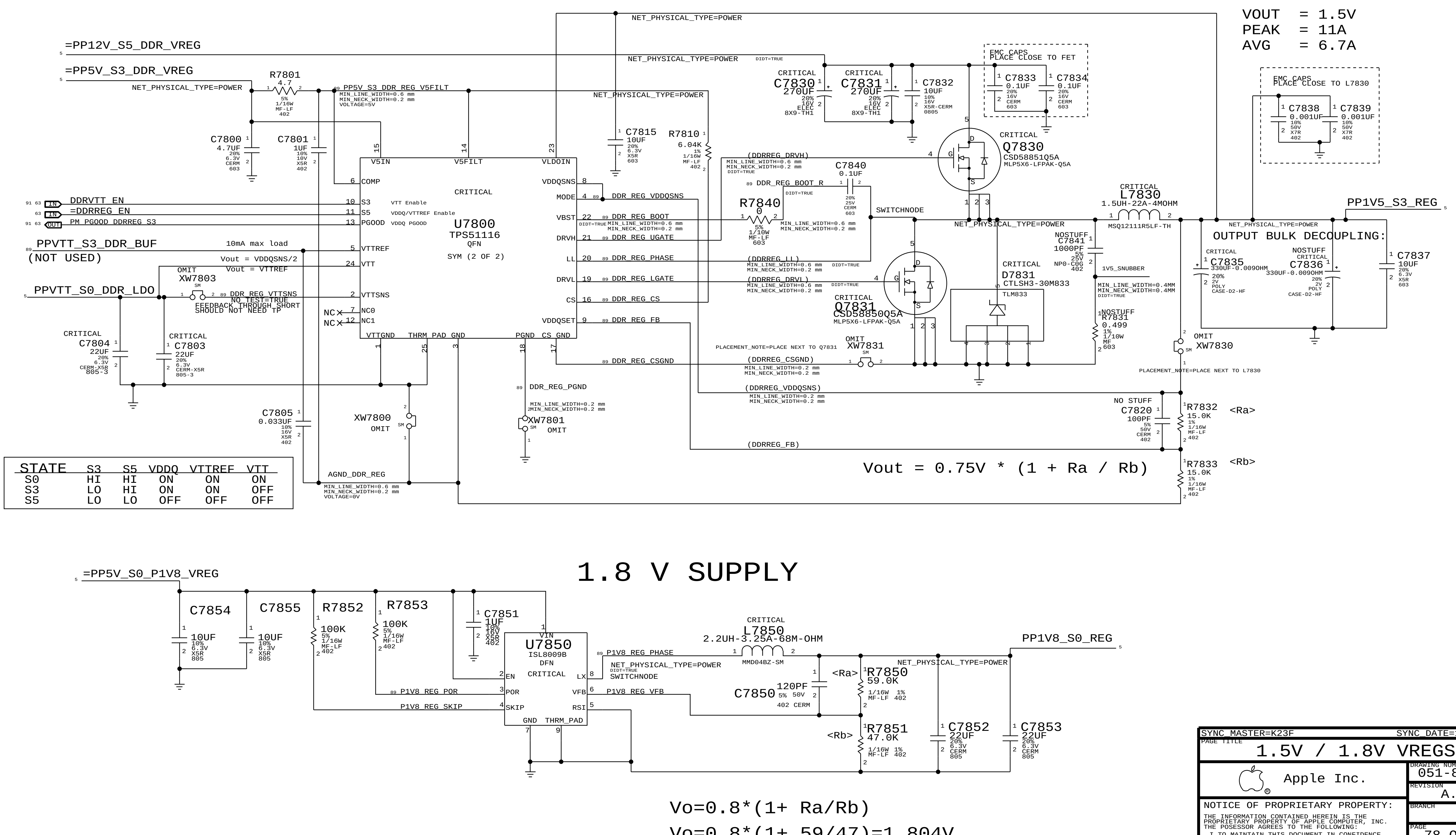
1.5 V DDR SUPPLY


PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A
=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
R7801 4.7
PP5V_S3_DDR_REG_V5FILT
C7800 4.7UF
C7801 1UF
U7800 TPS51116 QFN SYM (2 OF 2)
CRITICAL
V5IN
V5FILT
VLDOIN
COMP
VDDQSNS
MODE
VBST
DRVH
LL
DRVL
CS
VDDQSET
S3
S5
PGOOD
VTTREF
VTT
VTTSNS
NC0
NC1
VTTGND
THRM_PAD GND
PGND CS_GND
DDRVTT_EN
=DDRREG_EN
PM_PGOOD_DDRREG_S3
PPVTT_S3_DDR_BUF
(NOT USED)
10mA max load
Vout = VDDQSNS/2
Vout = VTTREF
PPVTT_S0_DDR_LDO
XW7803
FEEDBACK THROUGH SHORT
SHOULD NOT NEED TP
C7804 22UF
C7803 22UF
C7805 0.033UF
XW7800 OMIT
XW7801 OMIT
AGND_DDR_REG
DDR_REG_PGND
C7815 10UF
R7810 6.04K
C7830 270UF
C7831 270UF
C7832 10UF
EMC CAPS PLACE CLOSE TO FET
C7833 0.1UF
C7834 0.1UF
Q7830 CSD58851Q5A MLP5X6-LFPAK-Q5A
C7840 0.1UF
R7840 0
DDR_REG_BOOT_R
SWITCHNODE
L7830 1.5UH-22A-4MOHM MSQ12111R5LF-TH
C7841 1000PF
D7831 CTLSH3-30M833
Q7831 CSD58850Q5A MLP5X6-LFPAK-Q5A
XW7831
PLACEMENT_NOTE=PLACE NEXT TO Q7831
1V5_SNUBBER
R7831 0.499
NET_PHYSICAL_TYPE=POWER
OUTPUT BULK DECOUPLING:
C7835 330UF-0.009OHM
C7836 330UF-0.009OHM
C7837 10UF
EMC CAPS PLACE CLOSE TO L7830
C7838 0.001UF
C7839 0.001UF
PP1V5_S3_REG
XW7830 OMIT
PLACEMENT_NOTE=PLACE NEXT TO L7830
C7820 100PF
R7832 15.0K <Ra>
R7833 15.0K <Rb>
Vout = 0.75V * (1 + Ra / Rb)
(DDRREG_FB)
(DDRREG_CSGND)
(DDRREG_VDDQSNS)
1.8 V SUPPLY
=PP5V_S0_P1V8_VREG
C7854 10UF
C7855 10UF
R7852 100K
R7853 100K
C7851 1UF
U7850 ISL8009B DFN CRITICAL
EN
POR
SKIP
LX
VFB
RSI
GND THRM_PAD
P1V8_REG_PHASE
P1V8_REG_POR
P1V8_REG_SKIP
P1V8_REG_VFB
L7850 2.2UH-3.25A-68M-OHM MMD04BZ-SM
C7850 120PF
R7850 59.0K <Ra>
R7851 47.0K <Rb>
C7852 22UF
C7853 22UF
PP1V8_S0_REG
Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: 1.5V / 1.8V VREGS

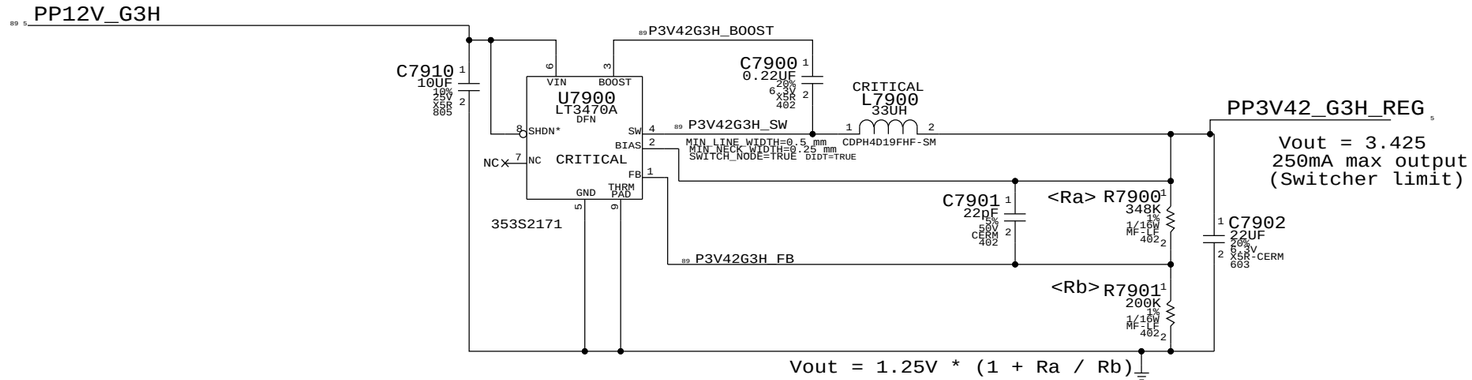
DRAWING NUMBER: 051-8337 SIZE: D

Apple Inc.

REVISION: A.0.0

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC MASTER=K74 MASTER SYNC DATE=N/A

PAGE TITLE: 3.42 G3HOT SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

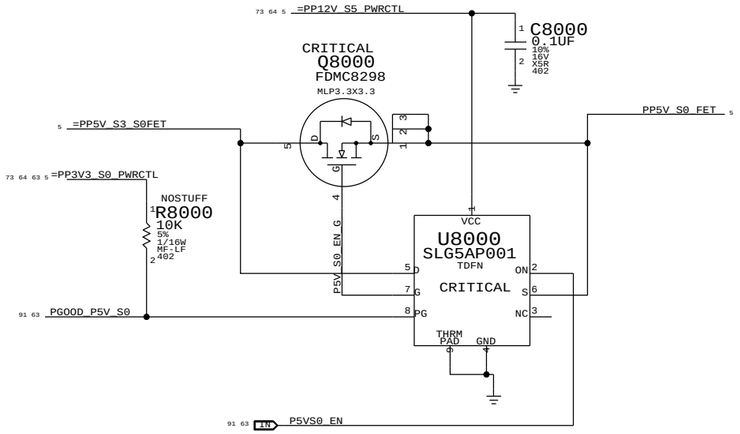
REVISION: A.0.0

BRANCH:

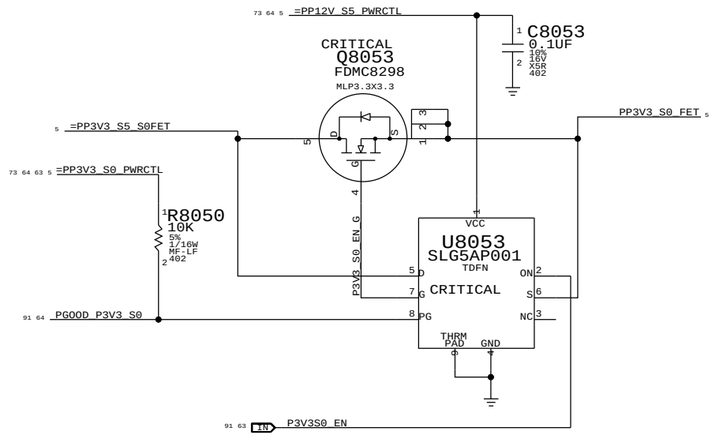
PAGE: 79 OF 110

SHEET: 72 OF 92

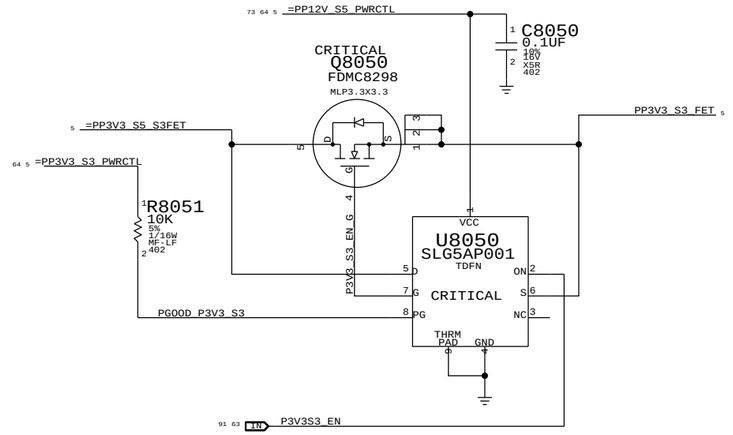
5V S0 FET (7A PK/2.7A AVG)



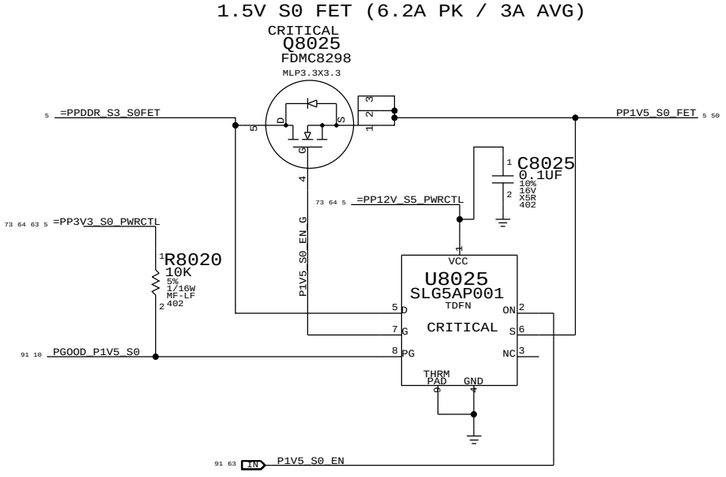
3.3V S0 FET (3.4APK / 1.9A AVG)



3.3V S3 FET (2.9A PK / 1.2A AVG)



1.5V S0 FET (6.2A PK / 3A AVG)



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: S3+S0 FETS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 80 OF 110

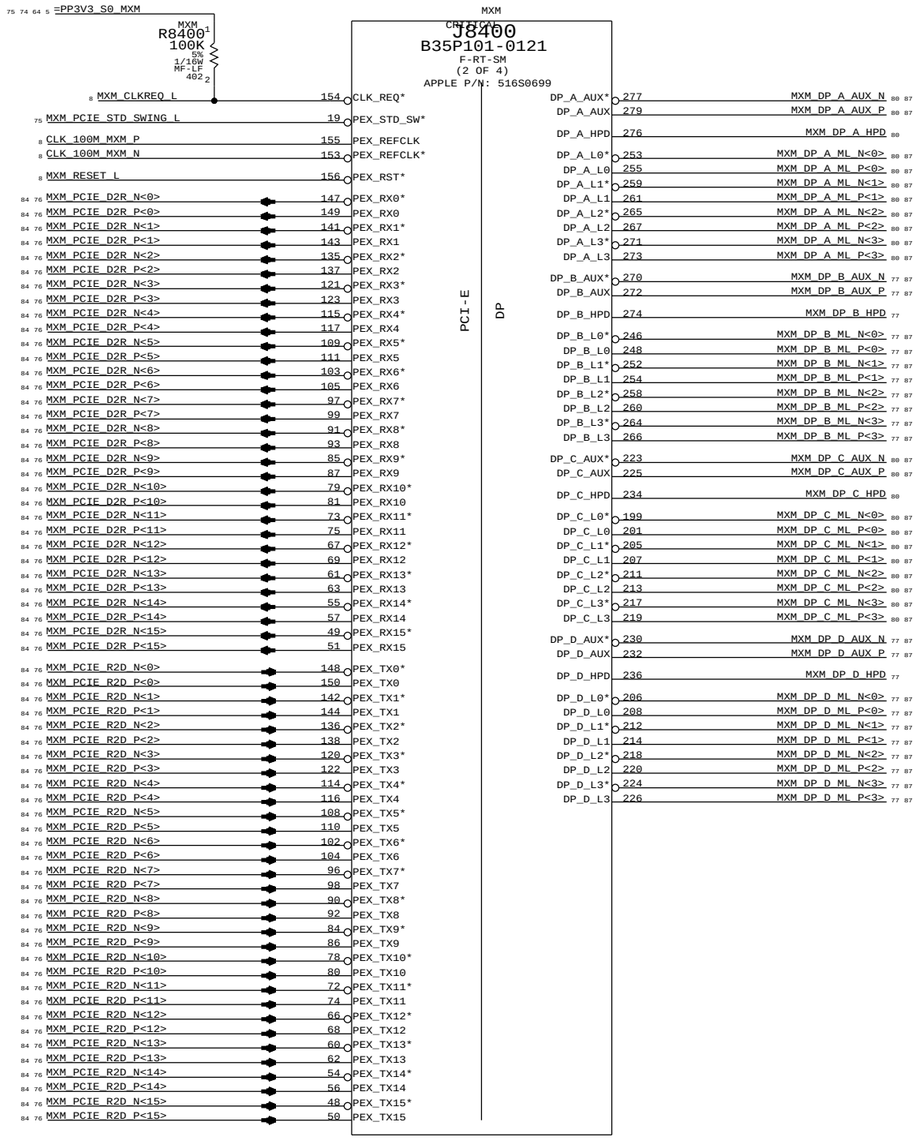
SHEET: 73 OF 92

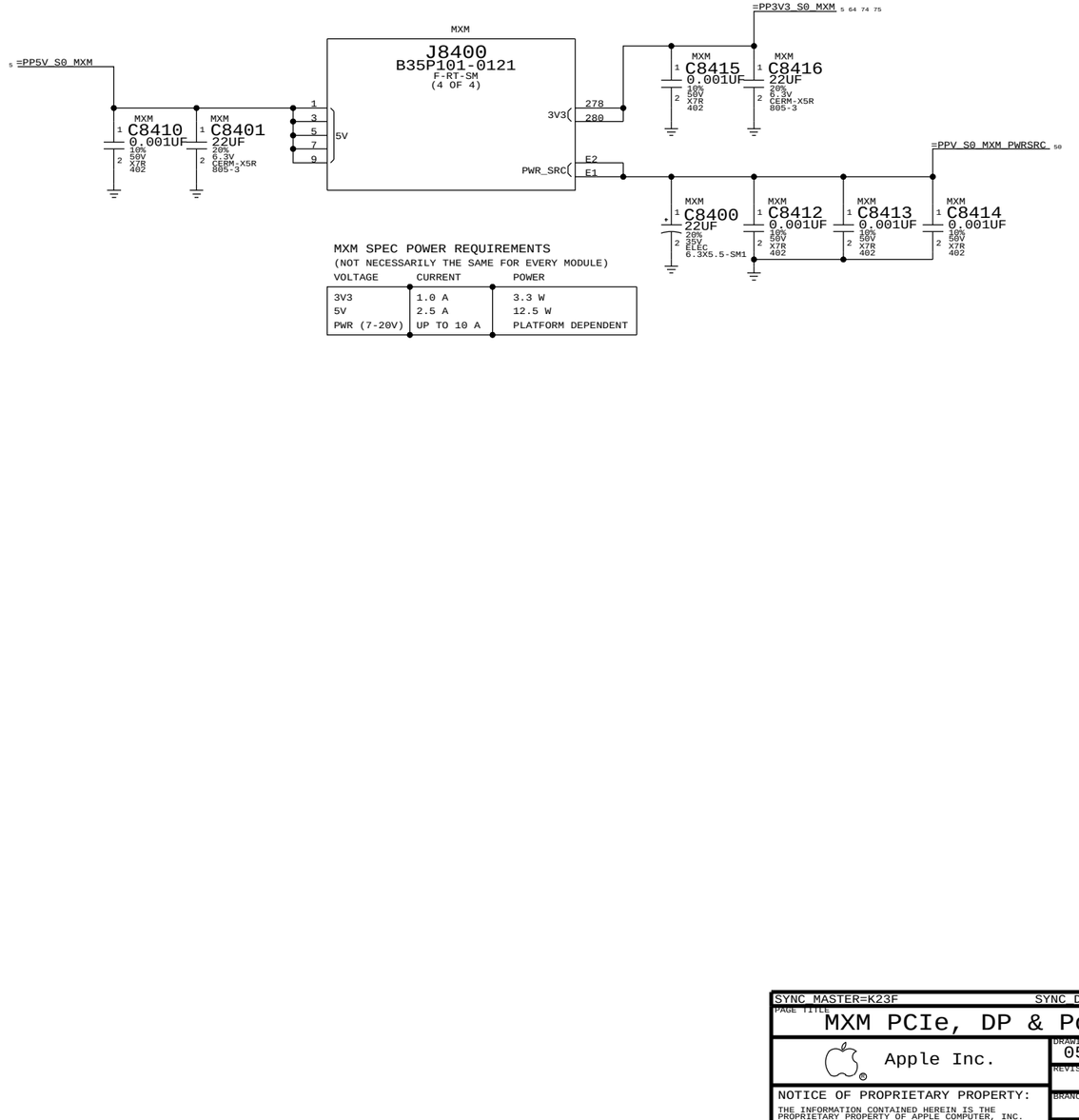
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 84 OF 110

SHEET: 74 OF 92

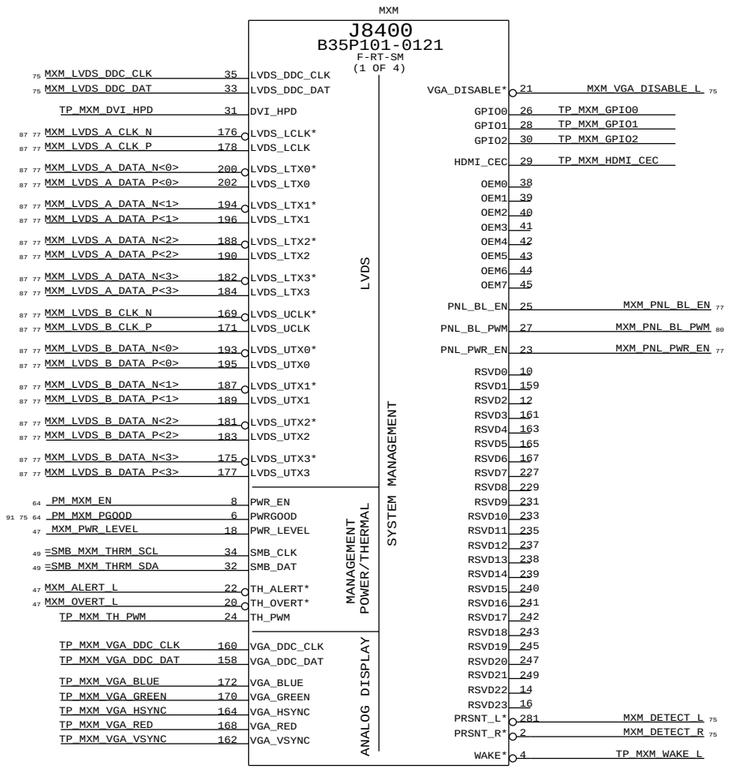
Page Notes

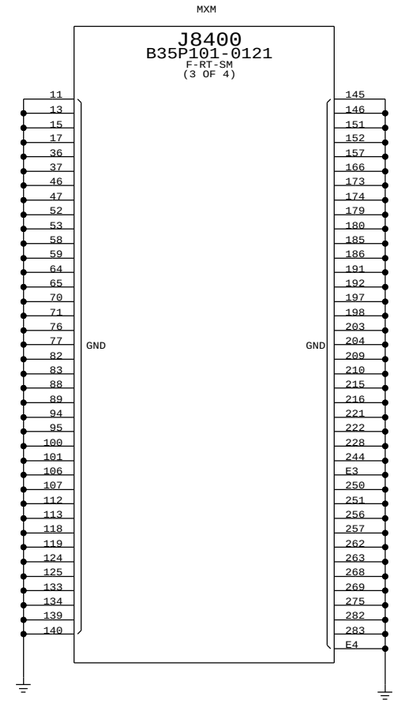
Power aliases required by this page:
- =PP3V3_S0_MXM

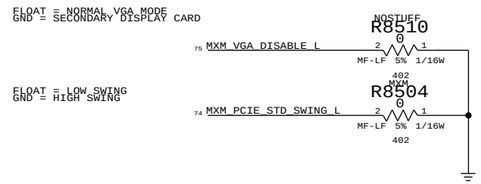
Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

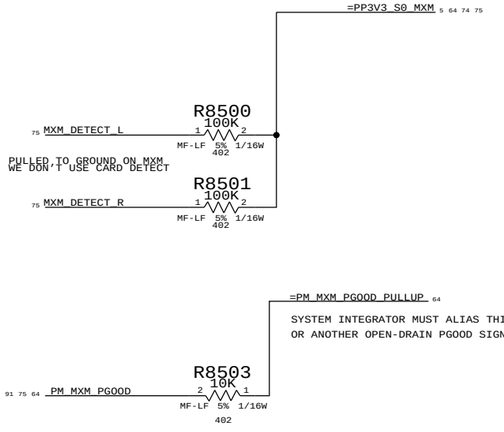
BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



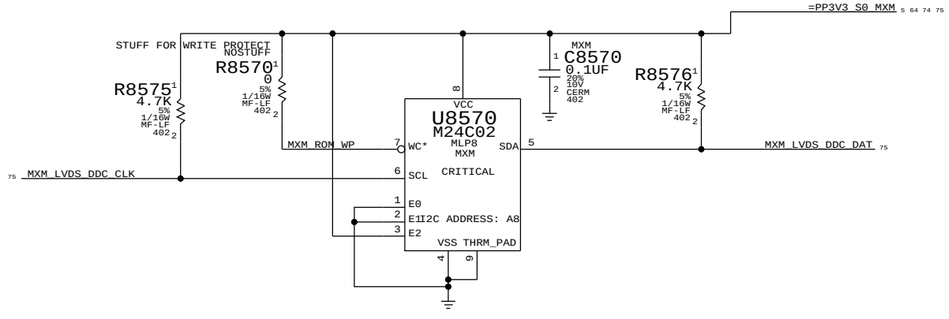






MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



SYNC_MASTER=K74_MASTER	SYNC_DATE=N/A
PAGE TITLE: MXM I/O	
Apple Inc.	DRAWING NUMBER: 051-8337 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 85 OF 110
	SHEET: 75 OF 92

MXM TX CAPS

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MXM RX CAPS

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SYNC_MASTER=K23F SYNC_DATE=11/30/2009

PAGE TITLE: MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

BRANCH:

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SHEET: 76 OF 92

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 75	MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM_LVDS_A_DATA_N<0>	NC_MXM_LVDS_A_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM_LVDS_A_DATA_P<0>	NC_MXM_LVDS_A_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM_LVDS_A_DATA_N<1>	NC_MXM_LVDS_A_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 75	MXM_LVDS_A_DATA_P<1>	NC_MXM_LVDS_A_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
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87 75	MXM_LVDS_A_DATA_P<2>	NC_MXM_LVDS_A_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
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87 75	MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
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87 75	MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 74	MXM_DP_B_ML_P<0..3>	NC_MXM_DP_B_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_B_AUX_P	NC_MXM_DP_B_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_B_AUX_N	NC_MXM_DP_B_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
74	MXM_DP_B_HPD	NC_MXM_DP_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_D_ML_P<0..3>	NC_MXM_DP_D_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_D_ML_N<0..3>	NC_MXM_DP_D_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_D_AUX_P	NC_MXM_DP_D_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_DP_D_AUX_N	NC_MXM_DP_D_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
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UNUSED MXM CONTROL SIGNALS

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75	MXM_PNL_PWR_EN	NC_MXM_PNL_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

DISPLAY AUDIO MUX NOT USED - SEND SPDIF TO CODEC

85 60	IN AUD_SPDIF_IN	AUD_SPDIF_IN_CODEC OUT	56 MAKE_BASE=TRUE
78	IN DP_INT_SPDIF_AUDIO	TP_DP_INT_SPDIF_AUDIO	MAKE_BASE=TRUE

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Display: Aliases

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 87 OF 110
SHEET: 77 OF 92

Page Notes

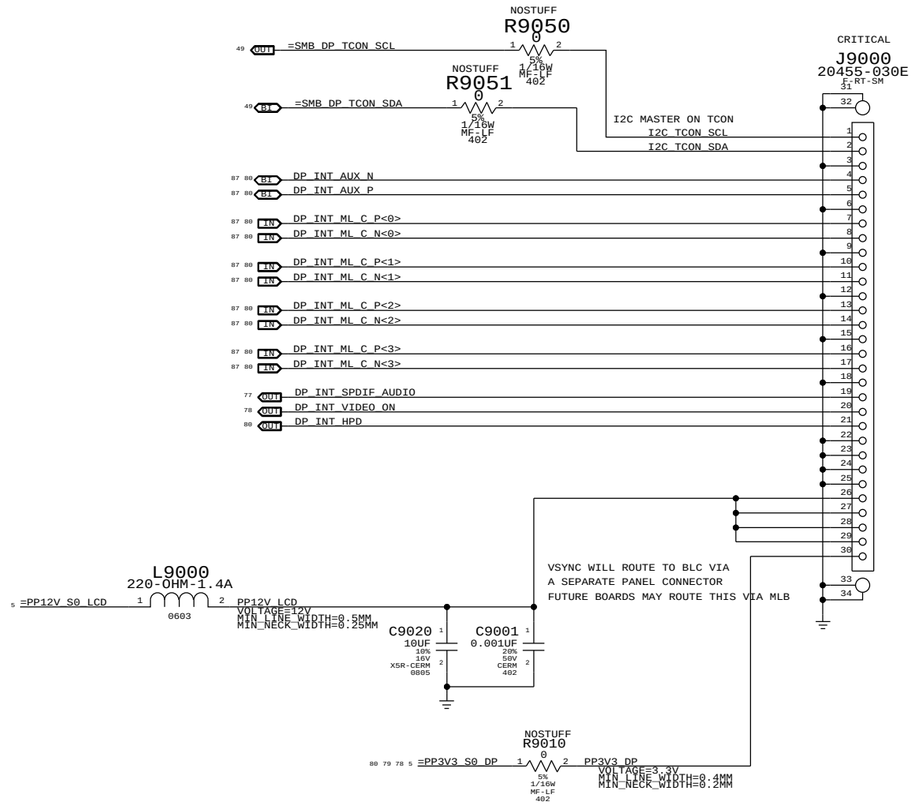
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_DP

Signal aliases required by this page:
- =SMB_DP_TCON_SCL, =SMB_DP_TCON_SDA

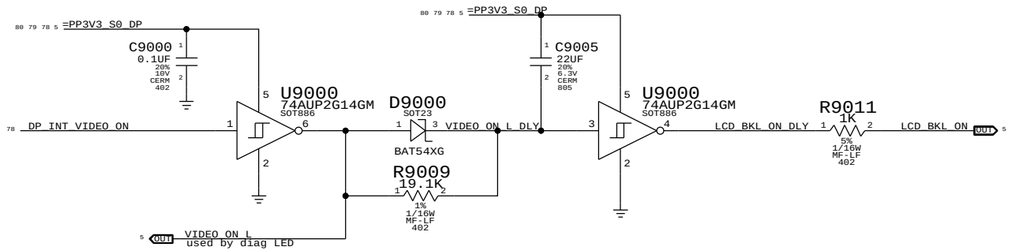
BOM options provided by this page:

INTERNAL DP INTERFACE



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
Display: Int DP Connector

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
REVISION A.0.0
BRANCH
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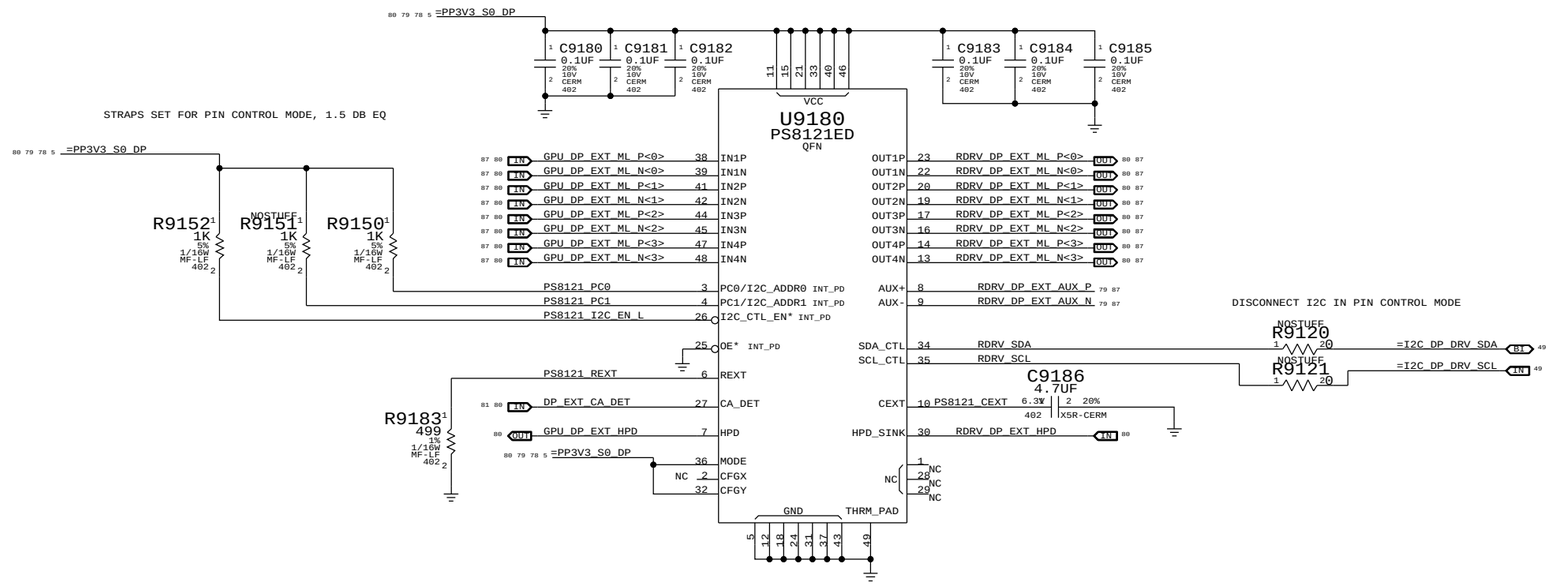
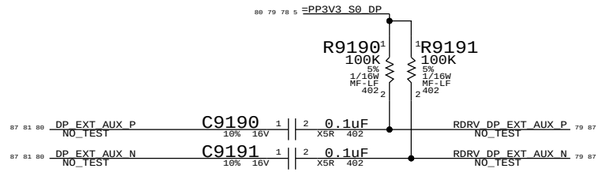
EQ & Re-Driver for DP source



COMMON MODE BIAS FOR PS8121ED AUX INTERCEPTION



SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE: DISPLAY: DP REDRIVER

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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FROM GPU TO REDRIVER

MXM_DP_A_ML_P<0>	NO_TEST	C9212	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<0>	87 74	IN	79 87
MXM_DP_A_ML_N<0>	NO_TEST	C9213	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<0>	87 74	IN	79 87
MXM_DP_A_ML_P<1>	NO_TEST	C9214	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<1>	87 74	IN	79 87
MXM_DP_A_ML_N<1>	NO_TEST	C9215	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<1>	87 74	IN	79 87
MXM_DP_A_ML_P<2>	NO_TEST	C9216	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<2>	87 74	IN	79 87
MXM_DP_A_ML_N<2>	NO_TEST	C9217	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<2>	87 74	IN	79 87
MXM_DP_A_ML_P<3>	NO_TEST	C9218	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_P<3>	87 74	IN	79 87
MXM_DP_A_ML_N<3>	NO_TEST	C9219	0.1uF 10% 16V X5R 402	NO_TEST	GPU_DP_EXT_ML_N<3>	87 74	IN	79 87

MXM_DP_A_HPD (74 OUT) = MAKE_BASE=TRUE = GPU_DP_EXT_HPD (IN 79)

REDRIVER TO EXTERNAL CONNECTOR

RDRV_DP_EXT_ML_P<0>	NO_TEST	C9230	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<0>	87 79	IN	81 87
RDRV_DP_EXT_ML_N<0>	NO_TEST	C9231	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<0>	87 79	IN	81 87
RDRV_DP_EXT_ML_P<1>	NO_TEST	C9232	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<1>	87 79	IN	81 87
RDRV_DP_EXT_ML_N<1>	NO_TEST	C9233	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<1>	87 79	IN	81 87
RDRV_DP_EXT_ML_P<2>	NO_TEST	C9234	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<2>	87 79	IN	81 87
RDRV_DP_EXT_ML_N<2>	NO_TEST	C9235	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<2>	87 79	IN	81 87
RDRV_DP_EXT_ML_P<3>	NO_TEST	C9236	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_P<3>	87 79	IN	81 87
RDRV_DP_EXT_ML_N<3>	NO_TEST	C9237	0.1uF 10% 16V X5R 402	NO_TEST	DP_EXT_ML_C_N<3>	87 79	IN	81 87

RDRV_DP_EXT_HPD (79 OUT) = MAKE_BASE=TRUE = DP_EXT_HPD (IN 81)

AUX/DDC SELECTION FOR EXTERNAL PORT

=PP3V3_S0_DP (80 79 78 5)

R9215 100K 5% 1/16W MF-LF 402 (1 2)

C9210 0.1UF 10% 16V X5R 402

MXM_DP_A_AUX_N (87 74 BI) — DP_EXT_AUX_N (BI 79 81 87)

=PP5V_S0_DP_AUX_MUX (80 5)

R9252 100K 5% 1/16W MF-LF 402

Q9250 SSM6N15FEAPE SOT563

DDC_CA_DET_LS5V

Q9251 SSM3K15FV SOD-VESM-HF

=PP5V_S0_DP_AUX_MUX (80 5)

R9202 100K 5% 1/16W MF-LF 402

DDC_CA_DET_LS5V_L

Q9201 SSM3K15FV SOD-VESM-HF

DP_EXT_CA_DET (81 79 IN)

Q9250 SSM6N15FEAPE SOT563

C9211 0.1UF 10% 16V X5R 402

MXM_DP_A_AUX_P (87 74 BI) — DP_EXT_AUX_P (BI 79 81 87)

R9216 100K 5% 1/16W MF-LF 402

GPU TO INTERNAL CONNECTOR

R9170 47 5% 1/16W MF-LF 402

CRITICAL L9170 FERR-220-OHM 0402

MXM_PNL_BL_PWM (75 IN) — LCD_PWM_FILT — LCD_PWM (OUT 5)

MXM_DP_C_ML_P<0>	NO_TEST	C9220	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<0>	87 74	IN	78 87
MXM_DP_C_ML_N<0>	NO_TEST	C9221	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<0>	87 74	IN	78 87
MXM_DP_C_ML_P<1>	NO_TEST	C9222	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<1>	87 74	IN	78 87
MXM_DP_C_ML_N<1>	NO_TEST	C9223	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<1>	87 74	IN	78 87
MXM_DP_C_ML_P<2>	NO_TEST	C9224	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<2>	87 74	IN	78 87
MXM_DP_C_ML_N<2>	NO_TEST	C9225	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<2>	87 74	IN	78 87
MXM_DP_C_ML_P<3>	NO_TEST	C9226	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_P<3>	87 74	IN	78 87
MXM_DP_C_ML_N<3>	NO_TEST	C9227	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_ML_C_N<3>	87 74	IN	78 87
MXM_DP_C_AUX_P	NO_TEST	C9200	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_AUX_P	87 74 BI	BI	78 87
MXM_DP_C_AUX_N	NO_TEST	C9201	0.1uF 10% 16V X5R 402	NO_TEST	DP_INT_AUX_N	87 74 BI	BI	78 87

R9200 100K 1% 1/16W MF-LF 402

R9201 100K 1% 1/16W MF-LF 402 — =PP3V3_S0_DP (5 78 79 80)

MXM_DP_C_HPD (74 OUT) = MAKE_BASE=TRUE = DP_INT_HPD (IN 78)

R9210 100K 1% 1/16W MF-LF 402

SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE: DISPLAYPORT CONNECTIONS

Apple Inc.

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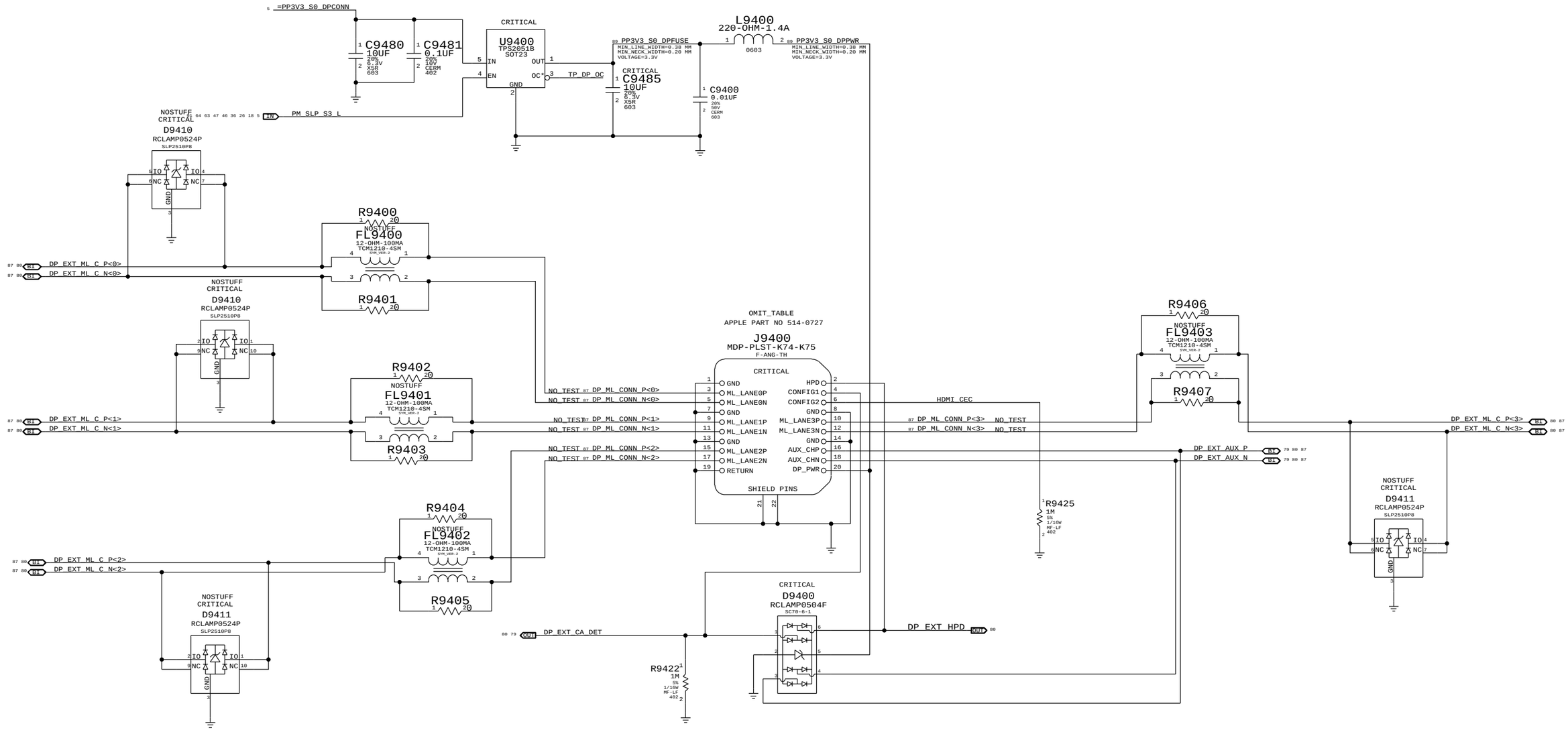

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0686	1	K22/K23 PROD. MDP	J9400	CRITICAL	METAL_IO
514-0727	1	K74/K75 MDP, PLASTIC, PD/NI	J9400	CRITICAL	PLASTIC_IO

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
Display: Ext DP Connector

Apple Inc.

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K74/K75 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
RCOMP	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
K74/K75 RULE DEFINITIONS

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	11 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	11 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	11 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	11 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	11 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	11 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	11 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	11 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	11 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	11 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	11 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	11 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	11 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	11 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	11 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	11 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	11 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	11 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	11 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	11 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	11 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	11 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	11 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	11 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	11 32

MEMORY POWER PROPERTIES

NET_TYPE

VOLTAGE	PHYSICAL	SPACING		
	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	11 28
	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	11 28

Memory Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	11 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	11 32
1.15V	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	10
1.15V	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	10
1.15V	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	10

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D

REVISION: A.0.0

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CPU ITP				
	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	10 24
	CPU_50S	CPU_ITP	CPU_CFG<17..0>	9 14 24
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0>	24
CPU_MISC				
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP	9
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_RBIAS	9
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP3	10
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP2	10
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP1	10
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_COMP0	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 76
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 76
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 76
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 76
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0>	74 76
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0>	74 76
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0>	74 76
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0>	74 76
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	17 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	17 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	9 18
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	9 18
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	9 18
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	9 18
FDI				
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	8
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	8
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	17 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	17 37
SATA				
	SATA_85D	SATA	SATA_HDD_R2D_C_P	17 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N	17 42
	SATA_85D	SATA	SATA_HDD_R2D_P	42
	SATA_85D	SATA	SATA_HDD_R2D_N	42
	SATA_85D	SATA	SATA_HDD_D2R_P	17 42
	SATA_85D	SATA	SATA_HDD_D2R_N	17 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P	42
	SATA_85D	SATA	SATA_HDD_D2R_C_N	42
	SATA_85D	SATA	SATA_ODD_R2D_C_P	17 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N	17 42
	SATA_85D	SATA	SATA_ODD_R2D_P	42
	SATA_85D	SATA	SATA_ODD_R2D_N	42
	SATA_85D	SATA	SATA_ODD_D2R_P	17 42
	SATA_85D	SATA	SATA_ODD_D2R_N	17 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P	42
	SATA_85D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P	10 24
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N	10 24
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P	17 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N	17 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P	17 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N	17 25
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P	17 25
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N	
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P	17 25
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N	17 25

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_REQ0_L	19
	PCI_55S	PCI	PCI_REQ1_L	19
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	19 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	17 27
	LPC_55S	LPC	LPC_AD<3..0>	17 46 48
	LPC_55S	LPC	LPC_FRAME_L	17 46 48
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	27 46
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 48
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R	8 18 91
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK	8 46 91
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	19 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	17 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	17 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	25
	CLK_XTAL	XTAL	CK505_XTAL_OUT	25
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	17 25
	USB_90D	USB	USB_HUB1_UP_P	19 34
	USB_90D	USB	USB_HUB1_UP_N	19 34
	USB_90D	USB	USB_HUB2_UP_P	19 35
	USB_90D	USB	USB_HUB2_UP_N	19 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_55S	SPI	SPI_CLK_R	17 48 55
	SPI_55S	SPI	SPI_CLK	55
	SPI_55S	SPI	SPI_MOSI_R	17 48 55
	SPI_55S	SPI	SPI_MOSI	55
	SPI_55S	SPI	SPI_MISO	17 48 55
	SPI_55S	SPI	SPI_MISO_R	55
	SPI_55S	SPI	SPI_CS0_R_L	17 48
	SPI_55S	SPI	SPI_CS0_L	48
	SPI_55S	SPI	SPI_MLB_CS_L	48 55
	SPI_55S	SPI	SPI_ALT_CS_L	48
	SPI_55S	SPI	SPIROM_USE_MLB	20 48
	SPI_55S	SPI	SPI_ALT_MOSI	48
	SPI_55S	SPI	SPI_ALT_MISO	48
	SPI_55S	SPI	SPI_ALT_CLK	48
	HDA_55S	HDA	HDA_BIT_CLK	17 56
	HDA_55S	HDA	HDA_BIT_CLK_R	17
	HDA_55S	HDA	HDA_RST_L	17 56
	HDA_55S	HDA	HDA_RST_R_L	17
	HDA_55S	HDA	HDA_SDOUT	17 56
	HDA_55S	HDA	HDA_SDOUT_R	17
	HDA_55S	HDA	HDA_SYNC	17 56
	HDA_55S	HDA	HDA_SYNC_R	17
	HDA_55S	HDA	HDA_SDIN0	17 56
	HDA_55S	HDA	AUD_SDI_R	56
		HDA	AUD_SPDIF_IN	60 77
		HDA	AUD_SPDIF_OUT	56 60
		HDA	AUD_SPDIF_CHIP	56
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_NOUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_POUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_NOUT	58 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_POUT	58 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_NOUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_POUT	59 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_NOUT	58 60 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_POUT	58 60 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	17 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	17 27
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	19
	PCH_55S	COMP_PCH	PCH_SATAICOMP	17
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	17
	PCH_55S	COMP_PCH	PCH_DMI_COMP	18
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_55S	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_55S	COMP_PCH	USB_HUB2_RBIAS	35

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE

IBEX PEAK CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

AUDIO CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=3:1_SPACING	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUD_DIFF	*	1:1_DIFFPAIR

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	ENET_50S	ENET_SE	BCM5764_RDAC 37
	ENET_50S	BUF0_CLK	BCM5764_CLK25M_XTALI 36 37
	ENET_50S	BUF0_CLK	BCM5764_CLK25M_XTALO 36 37
	ENET_50S	BUF0_CLK	BCM5764_CLK25M_XTAL 36
	ENET_100D	ENET_DIFF	ENET_MDI_P<3..0> 37 38
	ENET_100D	ENET_DIFF	ENET_MDI_N<3..0> 37 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_P<3..0> 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_N<3..0> 38
	ENET_100D	ENET_MII	PCIE_ENET_R2D_P 37
	ENET_100D	ENET_MII	PCIE_ENET_R2D_N 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_P 17 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_N 17 37
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_P 17 37
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_N 17 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_P 37
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_N 37
	SD_50S	SD	SDCONN_CMD 37 45
	SD_50S	SD	SDCONN_CLK 37 45
	SD_50S	SD	SDCONN_CLK_R 45
	SD_50S	SD	SDCONN_DATA<7..0> 37 45
	SD_50S	SD	BCM57765_CR_DATA<7..4> 37

FireWire Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW_PORT0_TPA_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_F_P 41
	FW_110D	FW_TP	FW_PORT0_TPA_F_N 41
	FW_110D	FW_TP	FW_PORT0_TPB_F_P 41
	FW_110D	FW_TP	FW_PORT0_TPB_F_N 41
PORT 1 & 2 NOT USED			
	FW_110D	FW_TP	FW_P0_TPA_L_P 40
	FW_110D	FW_TP	FW_P0_TPA_L_N 40
	FW_110D	FW_TP	FW_P0_TPB_L_P 40
	FW_110D	FW_TP	FW_P0_TPB_L_N 40
UNUSED FW NETS PHYSICAL PROPERTIES			
	FW_110D	FW_TP	FW_P1_TPA_P 39 40
	FW_110D	FW_TP	FW_P1_TPA_N 39 40
	FW_110D	FW_TP	FW_P2_TPA_P 39 40
	FW_110D	FW_TP	FW_P2_TPA_N 39 40

AUDIO NET PROPERTIES

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	AUD_DIFF	AUDIO	AUDAMPINBLN 58
	AUD_DIFF	AUDIO	AUDAMPINBLP 58
	AUD_DIFF	AUDIO	AUDAMPINLN 58
	AUD_DIFF	AUDIO	AUDAMPINLP 58
	AUD_DIFF	AUDIO	AUD_LO2_N_R 56 58
	AUD_DIFF	AUDIO	AUD_LO2_P_R 56 58
	AUD_DIFF	AUDIO	AUDAMPINBRN 58
	AUD_DIFF	AUDIO	AUDAMPINBRP 58
	AUD_DIFF	AUDIO	AUDAMPINRN 58
	AUD_DIFF	AUDIO	AUDAMPINRP 58
	AUD_DIFF	AUDIO	AUD_LO1_N_R 56 58
	AUD_DIFF	AUDIO	AUD_LO1_P_R 56 58
	AUD_DIFF	AUDIO	AUDAMPINCLN 59
	AUD_DIFF	AUDIO	AUDAMPINCLP 59
	AUD_DIFF	AUDIO	AUD_AMPINLN 59
	AUD_DIFF	AUDIO	AUD_AMPINLP 59
	AUD_DIFF	AUDIO	AUD_LO2_N_L 56 59
	AUD_DIFF	AUDIO	AUD_LO2_P_L 56 59
	AUD_DIFF	AUDIO	AUDAMPINCRN 59
	AUD_DIFF	AUDIO	AUDAMPINCRP 59
	AUD_DIFF	AUDIO	AUD_AMPINRN 59
	AUD_DIFF	AUDIO	AUD_AMPINRP 59
	AUD_DIFF	AUDIO	AUD_LO1_N_L 56 59
	AUD_DIFF	AUDIO	AUD_LO1_P_L 56 59

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE
ENET/SD/FW/AUD CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
ASSINGED IN CONT. MGR.			
111	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0> 74 80
111	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0> 74 80
	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0> 78 80
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P 74 80
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N 74 80
	DP_85D	DISPLAYPORT	DP_INT_AUX_P 78 80
	DP_85D	DISPLAYPORT	DP_INT_AUX_N 78 80
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_P<3..0> 74 80
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_N<3..0> 74 80
	DP_85D	DISPLAYPORT	GPU_DP_EXT_ML_P<3..0> 79 80
	DP_85D	DISPLAYPORT	GPU_DP_EXT_ML_N<3..0> 79 80
	DP_85D	DISPLAYPORT	RDRV_DP_EXT_ML_P<3..0> 79 80
	DP_85D	DISPLAYPORT	RDRV_DP_EXT_ML_N<3..0> 79 80
	DP_85D	DISPLAYPORT	DP_EXT_ML_C_P<3..0> 80 81
	DP_85D	DISPLAYPORT	DP_EXT_ML_C_N<3..0> 80 81
	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0> 81
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0> 81
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_P 74 80
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_N 74 80
	DP_85D	DISPLAYPORT	RDRV_DP_EXT_AUX_P 79
	DP_85D	DISPLAYPORT	RDRV_DP_EXT_AUX_N 79
	DP_85D	DISPLAYPORT	DP_EXT_AUX_P 79 80 81
	DP_85D	DISPLAYPORT	DP_EXT_AUX_N 79 80 81

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P 74 77
	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N 74 77
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P 74 77
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N 74 77
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P 75 77
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N 75 77
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P 75 77
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N 75 77
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0> 74 77
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0> 74 77
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0> 74 77
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0> 74 77
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0> 75 77
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0> 75 77
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0> 75 77
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0> 75 77

SYNC_MASTER=DAVE SYNC_DATE=01/07/2010

PAGE TITLE
GRAPHICS CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8337 SIZE D
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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL 49
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA 49
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL 49
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA 49
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL 49
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA 49
	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL 49
	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA 49
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL 49 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA 49 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL 49 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA 49 88
	SMB_5SS	SMB	SMBUS_PCH_CLK 17 49
	SMB_5SS	SMB	SMBUS_PCH_DATA 17 49
	SMB_5SS	SMB	SML_PCH_0_CLK 17 49
	SMB_5SS	SMB	SML_PCH_0_DATA 17 49
	SMB_5SS	SMB	SML_PCH_1_CLK 17 49
	SMB_5SS	SMB	SML_PCH_1_DATA 17 49
	CLK_XTAL	XTAL	SMC_EXTAL 46 47
	CLK_XTAL	XTAL	SMC_XTAL 46 47

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	THERM_DIFF	THERMAL	SNS_T1_DP1 52
	THERM_DIFF	THERMAL	SNS_T1_DN1 52
	THERM_DIFF	THERMAL	SNS_T1_DP2_DN3 44 52
	THERM_DIFF	THERMAL	SNS_T1_DN2_DP3 44 52
	THERM_DIFF	THERMAL	SNS_T2_DP1 52
	THERM_DIFF	THERMAL	SNS_T2_DN1 52
	THERM_DIFF	THERMAL	SNS_T2_DP2 52
	THERM_DIFF	THERMAL	SNS_T2_DN2 52
	THERM_DIFF	THERMAL	SNS_T2_DP3 52
	THERM_DIFF	THERMAL	SNS_T2_DN3 52
	THERM_DIFF	THERMAL	SNS_ODD_P 52 92
	THERM_DIFF	THERMAL	SNS_ODD_N 52 92
	THERM_DIFF	THERMAL	SNS_CPU_H_P 52
	THERM_DIFF	THERMAL	SNS_CPU_H_N 52
	THERM_DIFF	THERMAL	SNS_SKIN_P 52 92
	THERM_DIFF	THERMAL	SNS_SKIN_N 52 92
	THERM_DIFF	THERMAL	SNS_AMB_P 52 54 92
	THERM_DIFF	THERMAL	SNS_AMB_N 52 54 92
	THERM_DIFF	THERMAL	SNS_MXM_P 52
	THERM_DIFF	THERMAL	SNS_MXM_N 52
		THERMAL	HDD_OOB_TEMP_FILT 51 92
		THERMAL	HDD_OOB_TEMP 51
		THERMAL	HDD_OOB_TEMP_R 51
		THERMAL	SMC_HDD_OOB_TEMP 46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	THERM_DIFF	THERMAL	SENSE_MXM_P 50
	THERM_DIFF	THERMAL	SENSE_MXM_N 50
	THERM_DIFF	THERMAL	SENSE_VTT_R_P
	THERM_DIFF	THERMAL	SENSE_VTT_R_N
	THERM_DIFF	THERMAL	SENSE_CPU_1V5_P 50
	THERM_DIFF	THERMAL	SENSE_CPU_1V5_N 50
	THERM_DIFF	THERMAL	SENSE_CPU_VTT_P
	THERM_DIFF	THERMAL	SENSE_CPU_VTT_N
		THERMAL	GND_SMC_AVSS 46 47 50
		THERMAL	SMC_CPU_1V5_ISENSE 46 50
		THERMAL	SMC_CPU_1V5_ISENSE_R 50
		THERMAL	SMC_CPU_1V5_VSENSE 46 50
		THERMAL	SMC_CPU_VSENSE 46 50
	VID_PHY	VR_CTL	VR_CPU_IOUT 12 65
	THERM_DIFF	THERMAL	VR_ISNS_CPU_P 50
	THERM_DIFF	THERMAL	VR_ISNS_CPU_N 50
		THERMAL	SNS_PS_CPU_ISNS 50
		THERMAL	SMC_CPU_ISENSE 46 50

SYNC_MASTER=TEMP SYNC_DATE=12/09/2009

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: 051-8337 SIZE: D
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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
I128	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	66
I129	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	66
I130	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	66
I131	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	70
I132	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	70
I133	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE	
I134	POWER	SWITCHNODE	3.4V	P3V42G3H_SW	72
I136	POWER	SWITCHNODE	1.05V	PCHCORE_REG_PHASE	69
I137					
I138	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	71
I140	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	71
I141	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_A	28 30
I142	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_B	28 31
I144	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_A	28 30
I145	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_B	28 31
I147	POWER	POWER	12V	PP12V_AUD_SPKRAMP_PLANE	
I148	POWER	POWER	12V	PP12V_S0	5 64
I149	POWER	POWER	12V	PP12V_S0_CPU_FLTRD	65 66
I170	POWER	POWER	12V	PP12V_S0_FAN0_L	53 92
I171	POWER	POWER	12V	PP12V_S0_FAN1_L	53 92
I172	POWER	POWER	12V	PP12V_S0_FAN2_L	54 92
I660	POWER	POWER	12V	PP12V_G3H	5 72
I173	POWER	POWER	12V	PP12V_S5	5
I263	POWER	POWER	12V	FW_PORT0_VP	41
I272	POWER	POWER	12V	FW_PORT0_VP_F	41
I544	POWER	POWER	12V	PPVP_FW_PHY_CPS	40 41
I255	POWER	POWER	1.1V	PPVCORE_S0_CPU	5
I256	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	66
I562	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	66
I564	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	66
I177	POWER	POWER	1.05V	PP1V05_S0	5
I178	POWER	POWER	1.05V	PP1V05_S0_CK505_F	25
I179	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA	16 21
I180	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB	16 21
I181	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	
I182	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP	21 23
I183	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_FDI	21 23
I184	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA	21 23
I185	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK	21 23
I614	POWER	POWER	1.05V	PP1V05_SM_PCH_LAN	5
I265	POWER	POWER	1.1V	PPVTT_S0	5 50
I268	POWER	POWER	0.75V	PPVTT_S0_DDR	5
I613	POWER	POWER	0.75V	PP0V75_S0	5
I186	POWER	POWER	1.5V	PP1V5_S0	5
I187	POWER	POWER	1.5V	PP1V5_S0_CK505_F	25
I587	POWER	POWER	1.5V	PP1V5_S0_CK505_R	25
I189	POWER	POWER	1.5V	PP1V5_S3	5
I670	POWER	POWER	1.5V	PP1V5_CPU_MEM	5 50
I208	POWER	POWER	1.5V	PP1V8R1V5_S0_PCH_VCCVRM	21 23
I190	POWER	POWER	1.5V	PP1V5_FW_VDDA	39
I200	POWER	POWER	1.5V	PP1V8_S0	5
I206	POWER	POWER	1.96V	PP1V96_FW_PLLVDD	39
I205	POWER	POWER	1.96V	PP1V95_FW_FWPHY	39 40

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
I618	POWER	POWER	3.3V	PP3V3_S0	5
I219	POWER	POWER	3.3V	PP3V3_S0_CK505_F	25
I216	POWER	POWER	3.3V	PP3V3_S0_DPFUSE	81
I217	POWER	POWER	3.3V	PP3V3_S0_DPPWR	81
I222	POWER	POWER	3.3V	PP3V3_S0_HS_F	62
I223	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC	16 21
I620	POWER	POWER	3.3V	PP3V3_S0_TSENS_R	
I224	POWER	POWER	3.3V	PP3V3_S3	5 92
I657	POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
I246	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
I235	POWER	POWER	3.3V	PP3V3_S5	5
I677	POWER	POWER	3.3V	PPVTT_S3_DDR_BUF	71
I675	POWER	POWER	3.3V	PPV_S0_MXM_PWRSRC	60
I650	POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	21
I650	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUS	21
I650	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUSBYP	21
I262	POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	21
I641	POWER	POWER	3.3V	PPVOUT_S0_PCH_VCCRTC_NCTF	
I676	POWER	POWER	3.3V	PPVBATT_G3_RTC	27
I660	POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
I209	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	60 92
I209	POWER	POWER	3.3V	PP3V3_FW_AVDD	39
I210	POWER	POWER	3.3V	PP3V3_FW_ESD	41
I211	POWER	POWER	3.3V	PP3V3_FW_PLLVDD	39
I240	POWER	POWER	3.3V	PP3V3_FW_VDDA	39
I215	POWER	POWER	3.3V	PP3V3_G3_RTC	17 21 23 27
I213	POWER	POWER	3.3V	PP_ENET_CTRL12	36
I238	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	46
I231	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	46 47
I600	POWER	POWER	3.42V	PP3V42_G3H	5
I677	POWER	POWER	4.5V	4V5_REG_IN	56
I236	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	56
I237	POWER	POWER	5V	PP5V_S0	5 92
I239	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	65
I238	POWER	POWER	5V	PP5V_S0_PCH_V5REF	21 23
I240	POWER	POWER	5V	PP5V_S3	5 92
I242	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	71
I658	POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
I243	POWER	POWER	5V	PP5V_S3_IR_FLT	44 92
I244	POWER	POWER	5V	PP5V_S5	5
I245	POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	21 23
I247	POWER	POWER	5V	PP5V_USB2_PORT0	43
I247	POWER	POWER	5V	PP5V_USB2_PORT0_F	43
I248	POWER	POWER	5V	PP5V_USB2_PORT1	43
I248	POWER	POWER	5V	PP5V_USB2_PORT1_F	43
I249	POWER	POWER	5V	PP5V_USB2_PORT2	43
I249	POWER	POWER	5V	PP5V_USB2_PORT2_F	43
I250	POWER	POWER	5V	PP5V_USB2_PORT3	43
I250	POWER	POWER	5V	PP5V_USB2_PORT3_F	43
I648	POWER	POWER		DDR_REG_PGND	71
I648	POWER	POWER		DDR_REG_CSGND	71

SENSING NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
I156	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	65 66
I156	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	65 66
I157	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	65
I158	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	65
I160	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	65 66
I159	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	65 66
I161	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	65
I162	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	65
I163	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	65 66
I164	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	65 66
I165	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	65
I166	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	65
I150	SNS_DIFF		VR_CPU_VSEN	65
I668	SNS_DIFF		VR_CPU_RGND	65
I151	SNS_DIFF		VR_CPU_VSNS_R_N	65
I152	SNS_DIFF		VR_CPU_VSNS_R_P	65
I153	SNS_DIFF		VR_CPU_VSNS_XW_P	65
I155	SNS_DIFF		VR_CPU_VSNS_XW_N	65
I577	SNS_DIFF		CPU_VCC_PKG_SENSE_P	12 50 65
I576	SNS_DIFF		CPU_VCC_PKG_SENSE_N	12 65
I613	SNS_DIFF		VTT_REG_ISNS_P	
I616	SNS_DIFF		VTT_REG_ISNS_N	
I154	SNS_DIFF		CPU_VTTSENSE_P	12 68
I167	SNS_DIFF		CPU_VTTSENSE_N	12 68
I168	SNS_DIFF		CPU_VTTSENSE_R_P	
I174	SNS_DIFF		CPU_VTTSENSE_R_N	
I410	SNS_DIFF		VTT_REG_VSEN	
I410	SNS_DIFF		VTT_REG_RGND	
I617	SNS_DIFF		VTT_REG_RTO1	
I648	SNS_DIFF		VTT_REG_RTR1	

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
I278	VR_CTL_PHY	VR_CTL	VR_CPU_PH1_SNUB	66
I281	VR_CTL_PHY	VR_CTL	VR_CPU_PH2_SNUB	66
I285	VR_CTL_PHY	VR_CTL	VR_CPU_PH3_SNUB	66
I343	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	65 66
I344	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	65 66
I341	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	65
I342	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	65 66
I345	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	65
I346	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	65
I348	VR_CTL_PHY	VR_CTL	VR_CPU_REF	65
I349	VR_CTL_PHY	VR_CTL	VR_CPU_SS	65
I350	VR_CTL_PHY	VR_CTL	VR_CPU_TCOMP	65
I351	VR_CTL_PHY	VR_CTL	VR_CPU_TM	65
I352	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT1_RC	66
I353	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT2_RC	66
I354	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT3_RC	66
I355	VR_CTL_PHY	VR_CTL	VR_CPU_COMP	65
I356	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_R	65
I357	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_RC	65
I358	VR_CTL_PHY	VR_CTL	VR_CPU_DAC	65
I360	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_BOOT	66
I360	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	66
I360	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_LGATE	66
I360	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_UGATE	66
I360	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_BOOT	66
I362	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	66
I362	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_LGATE	66
I370	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_UGATE	66
I374	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_BOOT	66
I374	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	66
I374	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_LGATE	66
I374	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_UGATE	66
I381	VR_CTL_PHY	VR_CTL	VR_CPU_FAN	65
I381	VR_CTL_PHY	VR_CTL	VR_CPU_FB	65
I381	VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	65
I382	VR_CTL_PHY	VR_CTL	VR_CPU_FS	65
I382	VR_CTL_PHY	VR_CTL	VR_CPU_IMON	50 65
I383	VR_CTL_PHY	VR_CTL	VR_CPU_IOUT_PD	65
I382	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE	69
I384	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE	69
I385	VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB	69
I387	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON	69
I388	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP	69
I386	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT	69
I692	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R	69
I400	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT	
I400	VR_CTL_PHY	VR_CTL	VTT_REG_COMP	89
I400	VR_CTL_PHY	VR_CTL	VTT_REG_FB	
I400	VR_CTL_PHY	VR_CTL	VTT_REG_FS	
I400	VR_CTL_PHY	VR_CTL	VTT_REG_COMP	89
I400	VR_CTL_PHY	VR_CTL	VTT_REG_REF	89
I400	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE	
I410	VR_CTL_PHY	VR_CTL	VTT_REG_OCSET	
I411	VR_CTL_PHY	VR_CTL	VTT_OFS	
I411	VR_CTL_PHY	VR_CTL	VTT_REG_REF	89
I411	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE	
I410	VR_CTL_PHY	VR_CTL	VTT_REG_PH1_SNUB	
I600	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	72
I600	VR_CTL_PHY	VR_CTL	P3V42G3H_FB	72

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
I437	VR_CTL_PHY	VR_CTL	DDR_REG_CS	71
I438	VR_CTL_PHY	VR_CTL	DDR_REG_FB	71
I439	VR_CTL_PHY	SWITCHNODE	DDR_REG_LGATE	71
I440	VR_CTL_PHY	SWITCHNODE	DDR_REG_UGATE	71
I441	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT	71
I442	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT_R	71
I443	VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	71
I444	VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	71
I445	VR_CTL_PHY	VR_CTL	P1V8_REG_POR	71
I446	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT	70
I447	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT_R	70
I452	VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	70
I453	VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	70
I454	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_LGATE	70
I455	VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	70
I456	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_UGATE	70
I457	VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	70
I459	VR_CTL_PHY	VR_CTL	P5VS3_REG_BOOT	70
I460	VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	70
I462	VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	70
I463	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_LGATE	70
I465	VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	70
I466	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_UGATE	70

VR VID NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
I499	VID_PHY	VR_CTL	CPU_VID<0>	12 15 65
I499	VID_PHY	VR_CTL	CPU_VID<1>	12 15 65
I520	VID_PHY	VR_CTL	CPU_VID<2>	12 15 65
I522	VID_PHY	VR_CTL	CPU_VID<3>	12 15 65
I522	VID_PHY	VR_CTL	CPU_VID<4>	12 15 65
I522	VID_PHY	VR_CTL	CPU_VID<5>	12 15 65
I522	VID_PHY	VR_CTL	CPU_VID<6>	12 15 65
I520	VID_PHY	VR_CTL	CPU_VID<7>	12 15 65
I655	VID_PHY	VR_CTL	CPU_PSI_L	12 65

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	?

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

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POWER CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	PHYSICAL	SPACING		
T2	PM	PLT_RESET_L	19 27
T4	PM_VTT	PLT_RESET_LS1V1_L	10
T5	PM	PM_ACDC_PS_ON	5
T7	PM	PM_BATLOW_L	14 18 46
T8	PM	PM_CLK32K_SUSCLK	8 46 85
T9	PM	PM_CLK32K_SUSCLK_R	8 18 85
T6	PM	PM_CLKRUN_L	14 18 46 48
T10	PM	PM_EXT_TS_L<0>	
T11	PM	PM_EXT_TS_L<1>	
T12	PM	PM_LAN_PWRGD	14 18
T13	PM_VTT	FSB_CPURSTOUT_L	10 24
T25	PM_VTT	PM_MEM_PWRGD	10 18
T24	PM	PM_ME_PWRGD	18 64
T30	PM	PM_MXM_PGOOD	64 75
T20	PM	PM_PCH_PWRGD	18 64
T31	PM	PM_PGOOD_DDRREG_S3	63 71
T33	PM	PM_PGOOD_PVCORE_CPU	25 64 65
T32	PM	PM_PWRBTN_L	18 24 46
T35	PM	PM_RSMRST_L	46 63
T34	PM	PM_RSMRST_PCH_L	18 63
T36	PM	PM_SLP_M_L	18 63
T37	PM	PM_SLP_S3_L	5 18 26 36 46 47 63 64 81
T120	PM	PM_SLP_S4_1_L	18 63
T38	PM	PM_SLP_S4_L	18 47
T43	PM	PM_SLP_S5_L	18 47
T45	PM	PM_SUS_PWR_ACK	18
T22	PM_VTT	PM_SYNC	10 18
T199	PM	SDCARD_PLT_RST_L	27 44
T46	PM	PM_SYSRST_L	18 27 46
T44	PM	PM_SYS_PWRGD	18 64
T48	PM_VTT	PM_THRMTRIP_L	10 20 47
T49	PM	RSMRST_PWRGD	46 64
T47	PM	RTC_RESET_L	17 91
T50	PM_VTT	CPU_PWRGD	10 20 24
T40	PM	CPU_RESET_L	10 27
T55	PM	PGOOD_1V8_S0_G1	64
T56	PM	PGOOD_1V8_S0_G2	64
T54	PM	PGOOD_CPU_GFX_DDR	64
T57	PM	PGOOD_P1V5_S0	10 73
T58	PM	PGOOD_P1V8_S0	64
T60	PM	PGOOD_P3V3_S0	64 73
T61	PM	PGOOD_P3V3_S3	34 73
T62	PM	PGOOD_P5V_S0	63 73
T64	PM	PGOOD_PCH_AND_P1V8	64
T66	PM	PGOOD_PCH_S0	64
T65	PM	PGOOD_SYSPWROK	64
T67	PM	PGOOD_SYSPWROK_R	64
T68	PM	RTC_RESET_L	17 91
T69	PM	P12V_S3_EN	
T70	PM	P1V5_S0_EN	63 73
T74	PM	P3V3S0_EN	63 73
T75	PM	P3V3S3_EN	63 73
T76	PM	P5VS0_EN	63 73
T78	PM	P5VS3_EN	63 70
T77	PM	PCHCORE_REG_EN	63 69
T79	PM	PCHCORE_REG_PGOOD	63 64 69
T73	PM	PEG_RESET_L	8 27
T80	PM	SDCARD_RESET	20 44 92

	PHYSICAL	SPACING		
T82	PM	4V5_REG_EN	56
T81	PM	ALL_SYS_PWRGD_R	5 64
T84	PM	ALL_SYS_PWRGD_SMC	46 64
T83	PM	CK505_27MHZ_EN	25
T85	PM	CPUVTT_REG_EN	63 68
T86	PM_VTT	CPUVTT_REG_PGOOD	10 63 64 68
T87	PM	CPU_MEM_RESET_L	10 26
T88	PM	DDRVTT_EN	63 71
T89	PM	DEBUG_RESET_L	27 48
T90	PM	FWPHY_RESET_L	39
T91	PM	FWXIO_SNOOP_EN	39
T92	PM	FW_RESET_L	27 39
T95	PM	ENET_RESET_L	27 37
T97	PM	MEM_RESET_L	26 30 31
T98	PM	MINI_RESET_L	27 33
T99	PM	SMC_DELAYED_PWRGD	47 64
T100	PM	SMC_LRESET_L	27 46
T99	PM	SMC_RESET_L	46 47 48
T102	PM_VTT	XDP_CPUPWRGD	10 24
T101	PM_VTT	XDP_DBRESET_L	10 24 27
T103	PM_VTT	XDP_PWRGD	24

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

89 5 IN PP5V_S3 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
85 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
85 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE
85 44 IN USB_BT_L_P FUNC_TEST=TRUE
85 44 IN USB_BT_L_N FUNC_TEST=TRUE
49 44 IN =SMB_ALS_SCL FUNC_TEST=TRUE
49 44 IN =SMB_ALS_SDA FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

85 44 IN USB_SDCARD_L_P FUNC_TEST=TRUE
85 44 IN USB_SDCARD_L_N FUNC_TEST=TRUE
91 44 20 IN SDCARD_RESET FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

85 44 IN USB_IR_L_P FUNC_TEST=TRUE
85 44 IN USB_IR_L_N FUNC_TEST=TRUE
89 44 IN PP5V_S3_IR_FLT FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

88 52 IN SNS_ODD_P FUNC_TEST=TRUE
88 52 IN SNS_ODD_N FUNC_TEST=TRUE

J5600 ODD FAN

53 IN FAN_0_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH0_L FUNC_TEST=TRUE
89 53 IN PP12V_S0_FAN0_L FUNC_TEST=TRUE
53 IN FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

54 IN FAN_2_PWR_L FUNC_TEST=TRUE
54 IN FAN_TACH2_L FUNC_TEST=TRUE
89 54 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
54 IN FAN_2_GND FUNC_TEST=TRUE
88 54 52 IN SNS_AMB_P FUNC_TEST=TRUE
88 54 52 IN SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53 IN FAN_1_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH1_L FUNC_TEST=TRUE
89 53 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
53 IN FAN_1_GND FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

88 51 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

88 52 IN SNS_SKIN_P FUNC_TEST=TRUE
88 52 IN SNS_SKIN_N FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

60 IN AUD_MIC_IN1_N_CONN FUNC_TEST=TRUE
60 IN GND_AUDIO_MIC1_CONN FUNC_TEST=TRUE
60 IN AUD_MIC_IN1_P_CONN FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 60 58 IN AUD_SPKR_OUTLO2R_POUT FUNC_TEST=TRUE
85 60 58 IN AUD_SPKR_OUTLO2R_NOUT FUNC_TEST=TRUE
85 60 58 IN AUD_SPKR_OUTLO1R_POUT FUNC_TEST=TRUE
85 60 58 IN AUD_SPKR_OUTLO1R_NOUT FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 60 59 IN AUD_SPKR_OUTLO2L_POUT FUNC_TEST=TRUE
85 60 59 IN AUD_SPKR_OUTLO2L_NOUT FUNC_TEST=TRUE
85 60 59 IN AUD_SPKR_OUTLO1L_POUT FUNC_TEST=TRUE
85 60 59 IN AUD_SPKR_OUTLO1L_NOUT FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

89 60 IN PP3V3_AUDIO_SPDIF_JACK FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60 IN AUD_LI_DET_JACK FUNC_TEST=TRUE
60 IN AUD_LI_R_JACK FUNC_TEST=TRUE
60 IN AUD_LI_GND_JACK FUNC_TEST=TRUE
60 IN AUD_LI_L_JACK FUNC_TEST=TRUE
60 IN HS_MIC_LO_JACK FUNC_TEST=TRUE
60 IN HS_MIC_HI_JACK FUNC_TEST=TRUE
60 IN AUD_HP_L_JACK FUNC_TEST=TRUE
60 IN AUD_HP_GND_JACK FUNC_TEST=TRUE
60 IN AUD_HP_R_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TYPEDET_JACK FUNC_TEST=TRUE
60 IN AUD_IP_PERPH_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TIPDET_JACK FUNC_TEST=TRUE
60 IN AUD_SPDIFIN_JACK FUNC_TEST=TRUE
60 IN AUD_SPDIF_OUT_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

GND 17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17
89 5 IN PP3V3_S3 2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
70 5 IN PP5V_S3_REG 1 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
89 5 IN PP5V_S0 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

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